

**CC Technical Documentation**  
**RM-11 Series Transceivers**

# **Troubleshooting – Baseband**

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## Troubleshooting Overview

The baseband module of the RM-11 transceiver is a trimode, CDMA, dual-band engine and consists of three main Application Specific Integrated Circuits (ASICs):

- Universal Energy Management (UEM)
- Universal Phone Processor (UPP)
- A 128-Megabit FLASH

The baseband architecture is based on the DCT4 Apollo engine and supports a power-saving function called *sleep mode*. Sleep mode shuts off the VCTCXO, which is used as a system clock source for both the RF and the baseband. The phone awakens by a timer running from this 32 kHz clock. The sleep time is determined by network parameters. During the sleep mode, the system runs from a 32 kHz crystal. Sleep mode is entered when both the MCU and the DSP are in standby mode, and the 19.2 MHz Clk (VCTCXO) is switched off.

The RM-11 supports both two and three DCT3 type wire chargers. However, the 3-wire chargers are treated as two-type wire chargers. Charging is controlled by the UEM ASIC and EM SW.

A BLD-3 Li-ion battery is used as the main power source. The BLD-3 has a nominal capacity of 780 mAh.

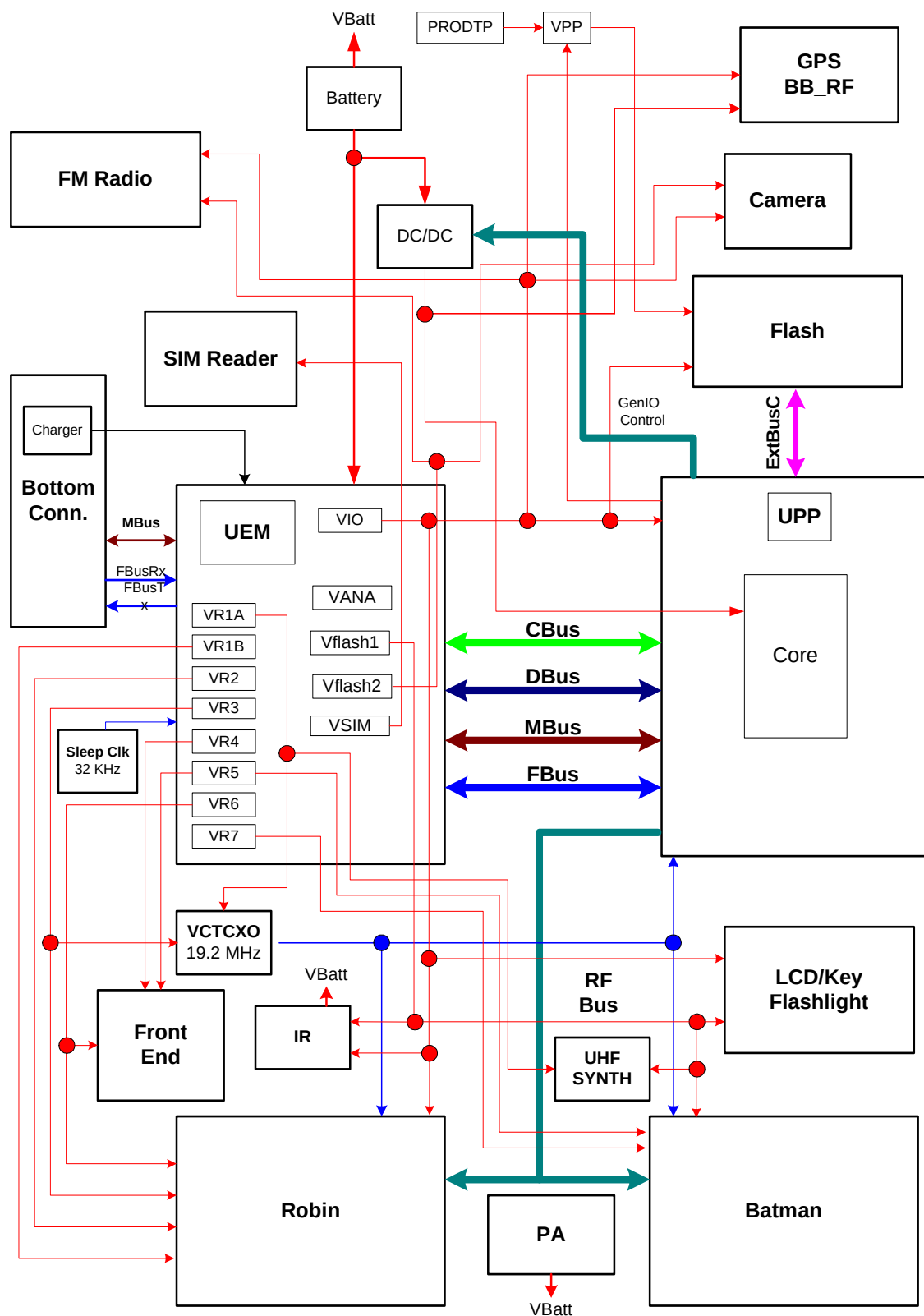


Figure 1: RM-11 power distribution

## Power Up and Reset

Power up and reset are controlled by the UEM ASIC. The RM-11 baseband can be powered up in the following ways:

- By the Power button, which means grounding the PWRONX pin of the UEM
- By connecting the charger to the charger input
- By the RTC alarm, when the RTC logic has been programmed to give an alarm

After receiving one of the above signals, the UEM counts a 20ms delay and enters into reset mode. The watchdog starts up, and if the battery voltage is greater than  $V_{\text{coff+}}$ , a 200ms delay starts to allow references (etc.) to settle. After this delay elapses, the VFLASH1 regulator is enabled. Then, 500us later the VR3, VANA, VIO, and VCORE are enabled. Finally, the power-up reset (PURX) line is held low for 20 ms. The PURX reset is fed to the baseband UPP ASIC. Resets are generated for the MCU and the DSP. During this reset phase, the UEM forces the VCTCX0 regulator on — regardless of the status of the sleep control input signal — to the UEM. The FLSRSTx from the ASIC is used to reset the flash during power up and to put the flash in power down during sleep. All baseband regulators are switched on when the UEM powers on. The UEM internal watchdogs are running during the UEM reset state, with the longest watchdog time selected. If the watchdog expires, the UEM returns to the power-off state. The UEM watchdogs are internally acknowledged at the rising edge of the PURX signal in order to always give the same watchdog response time to the MCU.

Figure 2 represents the UEM start-up sequence from reset to power-on modes.

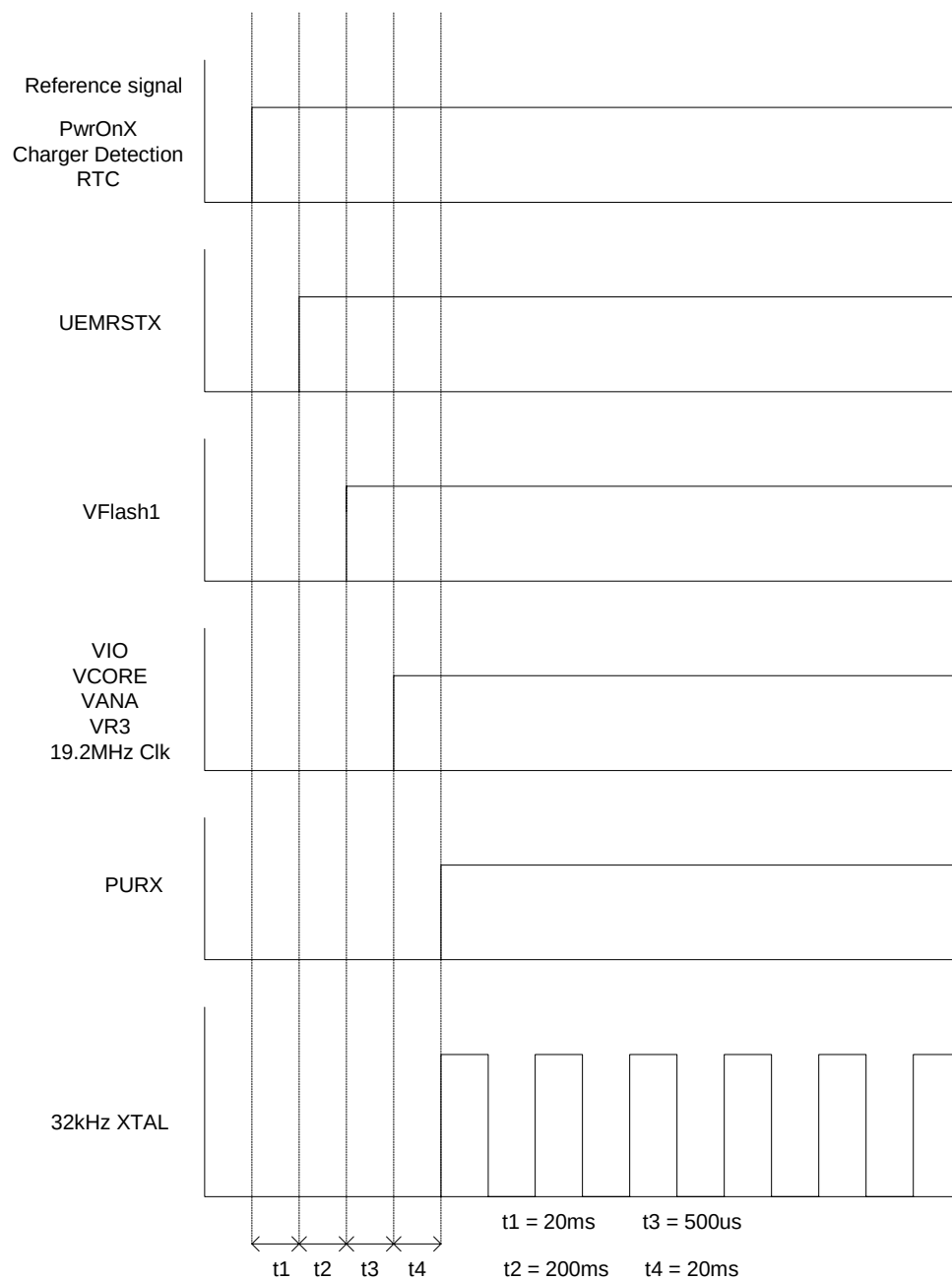


Figure 2: UEM start-up sequence from reset to power-on mode

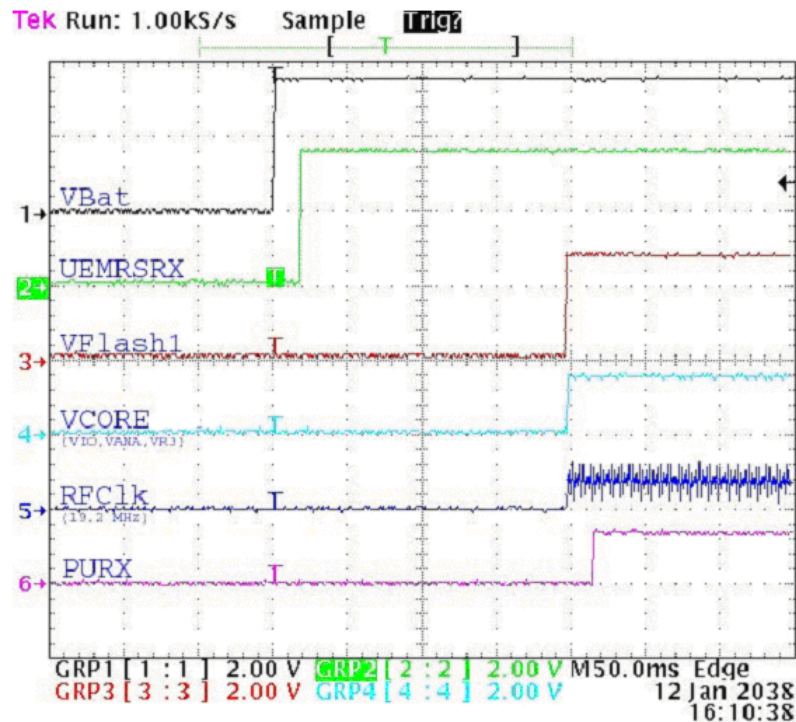


Figure 3: Power up

### Power Up – Power Key

When the Power key is pressed, the UEM enters the power up sequence. Pressing the Power key causes the PWRONX pin on the UEM to be grounded. The UEM PWRONX signal is not part of the keypad matrix. The Power key is only connected to the UEM. This means that when pressing the power key, an interrupt is generated to the UPP that starts the MCU. The MCU then reads the UEM interrupt register and notices that it is a PWRONX interrupt. Then the MCU reads the status of the PWRONX signal using the UEM control bus (CBUS). If the PWRONX signal stays low for a specific duration, the MCU accepts this as a valid power on state and continues with the SW initialization of the baseband. If the power on key does not indicate a valid power on situation, the MCU powers off the baseband.

### Power Up – Charger

In order to be able to detect and start charging in the case where the main battery is fully discharged (empty) and hence the UEM has no supply (NO\_SUPPLY or BACKUP mode of UEM), charging is controlled by START-UP CHARGING circuitry.

Whenever a VBAT level is detected to be below the master reset threshold (VMSTR-), charging starts and is controlled by START\_UP charge circuitry. Connecting a charger forces the VCHAR input to rise above the charger detection threshold (VCHDET+) and by detection charging is started. The UEM generates 100 mA constant output current from the connected charger's output voltage. The battery's voltage rises as it charges, and when the VBAT voltage level is detected to be higher than the master reset threshold limit (VMSTR+), the START\_UP charge is terminated.

Monitoring the VBAT voltage level is done by the charge control block (CHACON). A MSTRX='1' output reset signal (internal to the UEM) is given to the UEM's RESET block when the  $VBAT > VMSTR+$  and UEM enter into the reset sequence.

If VBAT is detected to fall below VMSTR- during start-up charging, charging is cancelled. It will restart if new rising edge on the VCHAR input is detected (VCHAR rising above VCH-ET+).

### Power Up – RTC Alarm

If phone is in POWER\_OFF mode when an RTC alarm occurs, a wake-up procedure begins. After the baseband is powered ON, an interrupt is given to the MCU. When an RTC alarm occurs during ACTIVE mode, an interrupt is generated to the MCU.

### Power Off

The baseband switches into power off mode if any of following occurs:

- Power key is pressed
- Battery voltage is too low ( $VBATT < 3.2\text{ V}$ )
- Watchdog timer register expires

The UEM controls the power down procedure.

### Power Consumption and Operation Modes

During power off mode, power (VBAT) is supplied to the UEM, BUZZER, VIBRA, LED, PA, and PA drivers (Tomcat and Hornet). During this mode, the current consumption is approximately 35  $\mu\text{A}$ , which is the UEM leakage current.

In sleep mode, both processors (MCU and DSP) are in stand-by mode. The phone enters sleep mode only when both processors make this request. When the SLEEPX signal is detected low by the UEM, the phone enters SLEEP mode. The VIO and VFLASH1 regulators are put into low quiescent current mode, VCORE enters LDO mode, and the VANA and VFLASH2 regulators are disabled. All RF regulators are disabled during SLEEP mode. When the UEM detects a high SLEEPX signal, the phone enters ACTIVE mode and all functions are activated.

The sleep mode is exited either by the expiration of a sleep clock counter in the UEM or by some external interrupt (a charger connection, key press, headset connection, etc.).

In sleep mode, the VCTCXO (19.2 MHz Clk) is shut down and the 32 kHz sleep clock oscillator is used as a reference clock for the baseband.

The average current consumption of the phone can vary depending mainly on the SW state (e.g., slot cycle 0, 1, or 2) and if the phone is working on IS95 or IS2000 for CDMA. However, the average consumption is about 6 mA in slot cycle 0 on IS95.

In the ACTIVE mode, the phone is in normal operation; scanning for channels, listening to a base station, and transmitting and processing information. There are several sub-states in the active mode depending on the phone's present state, such as burst reception, burst transmission, if DSP is working, etc.

In active mode, SW controls the UEM RF regulators: VR1A and VR1B can be enabled or disabled. These regulators work of the UEM charge pump. VSIM can be enabled or disabled and its output voltage can be programmed to be 1.8 V or 3.3 V. VR2 and VR4–VR7 can be enabled, disabled, or forced into low quiescent current mode. VR3 is always enabled in active mode and disabled during sleep mode and cannot be controlled by SW in the same way as the other regulators. VR3 will only turn off if both processors (DSP and MCU) request to be in sleep mode.

CHARGING mode can be performed in parallel with any other operating mode. A BSI resistor inside the battery indicates the battery type/size. The resistor value corresponds to a specific battery type and capacity. This capacity value is related to the battery technology.

The battery voltage, temperature, size and charging current are measured by the UEM, and the EM charging algorithm controls it.

The charging control circuitry (CHACON) inside the UEM controls the charging current delivered from the charger to the battery. The battery voltage rise is limited by turning the UEM switch off when the battery voltage reaches 4.2 V. The charging current is monitored by measuring the voltage drop across a 220 mOhm resistor.

## Power

In normal operation, the baseband is powered from the phone's battery. The battery consists of one Lithium-Ion cell. In the case of RM-11, the battery capacity is 780 mAh.

The UEM ASIC controls the power distribution to the whole phone through the BB and RF regulators excluding the power amplifier (PA) and the DC/DC, which have a continuous power rail directly from the battery. The battery feeds power directly to the following parts of the system:

- UEM
- PA
- DC/DC
- Buzzer
- Vibra
- Display and keyboard lights

The UEM is the heart of the power distribution to the phone, which includes all the voltage regulators. The UEM handles power-up hardware functions so the regulators are not powered and the power-up reset (PURX) is not released if the battery voltage is less than 2.8 V.

The RM-11 baseband is powered from five different UEM regulators:

**Table 1: RM-11 Baseband Regulators**

| Regulator   | Maximum current (mA) | Vout (V) | Notes                                                                              |
|-------------|----------------------|----------|------------------------------------------------------------------------------------|
| VCORE DD/DC | 300                  | 1.5      | Output voltage selectable 1.0V/1.3V/1.5V/1.8V<br>Default power at power-up is 1.5V |
| VIO         | 150                  | 1.8      | Enabled always except during power-off mode                                        |
| VFLASH1     | 70                   | 2.78     | Enabled always except during power-off mode                                        |
| VFLASH2     | 40                   | 2.78     | Enabled only when data cable is connected                                          |
| VANA        | 80                   | 2.78     | Enabled only when the system is awake (off during sleep and power-off modes)       |
| VSIM        | 25                   | 3.0      | Not used                                                                           |

Table 2 includes the UEM voltage regulators used by the RF.

**Table 2: RM-11 RF Regulators**

| Regulator | Maximum current (mA) | Vout (V) | Notes                              |
|-----------|----------------------|----------|------------------------------------|
| VR1A      | 10                   | 4.75     | Enabled when the receiver is on    |
| VR1B      | 10                   | 4.75     | Enabled when the transmitter is on |
| VR2       | 100                  | 2.78     | Enabled when the transmitter is on |
| VR3       | 20                   | 2.78     | Enabled when SleepX is high        |
| VR4       | 50                   | 2.78     | Enabled when the receiver is on    |
| VR5       | 50                   | 2.78     | Enabled when the receiver is on    |
| VR6       | 50                   | 2.78     | Enabled when the transmitter is on |
| VR7       | 45                   | 2.78     | Enabled when the receiver is on    |

A charge pump used by VR1A is constructed around the UEM. The charge pump works with Cbus (1.2 MHz Clk) and gives a 4.75 V regulated output voltage to the RF.

## Clock Distribution

### RFCIk (19.2 MHz Analog)

The baseband's main clock signal is generated from the VCTCXO (G503). This 19.2 MHz clock signal is generated at the RF and fed to the UPP's RFCLK pin.

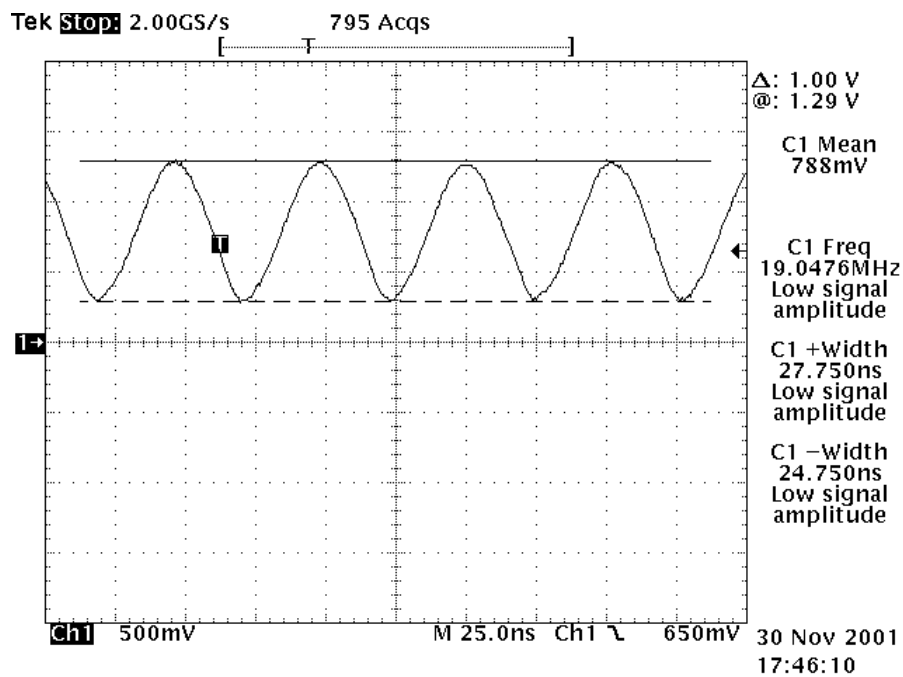


Figure 4: 19.2 MHz analog

### RFConvClk (19.2 MHz Digital)

The UPP distributes the 19.2 MHz Clk to the internal processors, DSP, and MCU, where SW multiplies this clock by seven for the DSP and by two for the MCU.

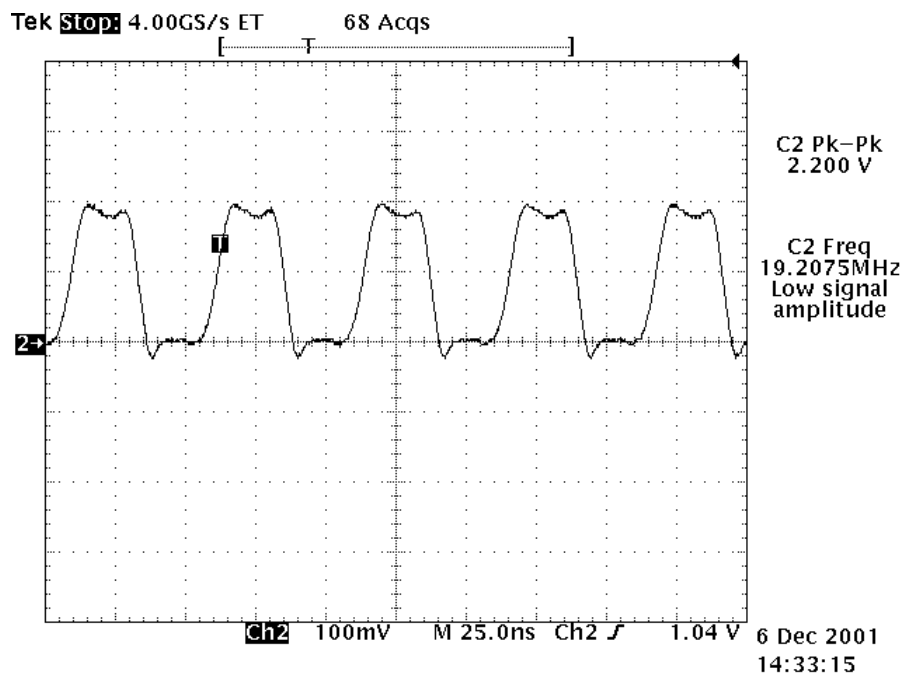


Figure 5: 19.2 MHz digital

### CBUSClk Interface

A 1.2 MHz clock signal is used for CBUS, which is used by the MCU to transfer data between the UEM and UPP.

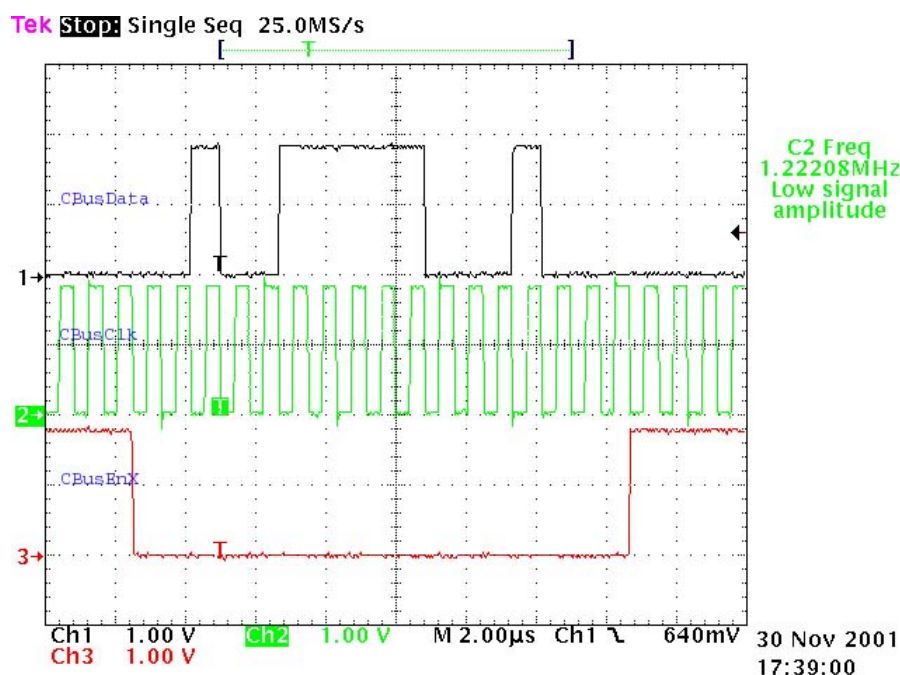


Figure 6: 1.2 MHz CBUS clock signal

### DBUS Clk Interface

A 9.6 MHz clock signal is used for DBUS, which is used by the DSP to transfer data between the UEM and the UPP.

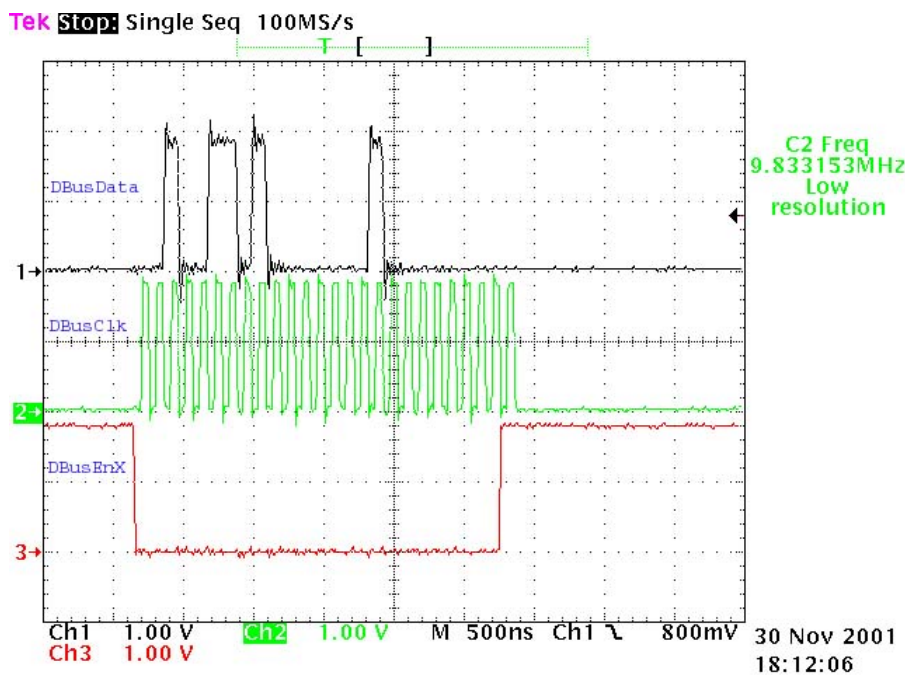


Figure 7: 9.6 MHz clock signal

The system clock can be stopped during sleep mode by disabling the VCTCX0 power supply from the UEM regulator output (VR3) by turning off the controlled output signal SLEEPX from the UPP.

### SleepCLK (Digital)

The UEM provides a 32 kHz sleep clock for internal use and to the UPP, where it is used for the sleep mode timing.

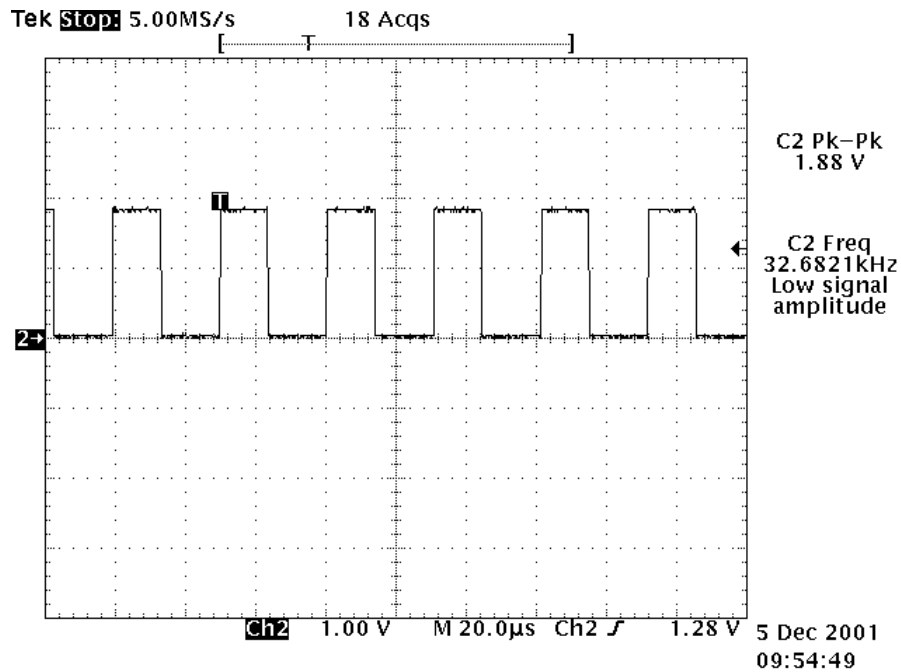


Figure 8: 32 kHz digital sleep clock signal

## SleepCLK (Analog)

When the system enters sleep mode or power off mode, the external 32 KHz crystal provides a reference to the UEM RTC circuit to turn on the phone during power off or sleep mode.

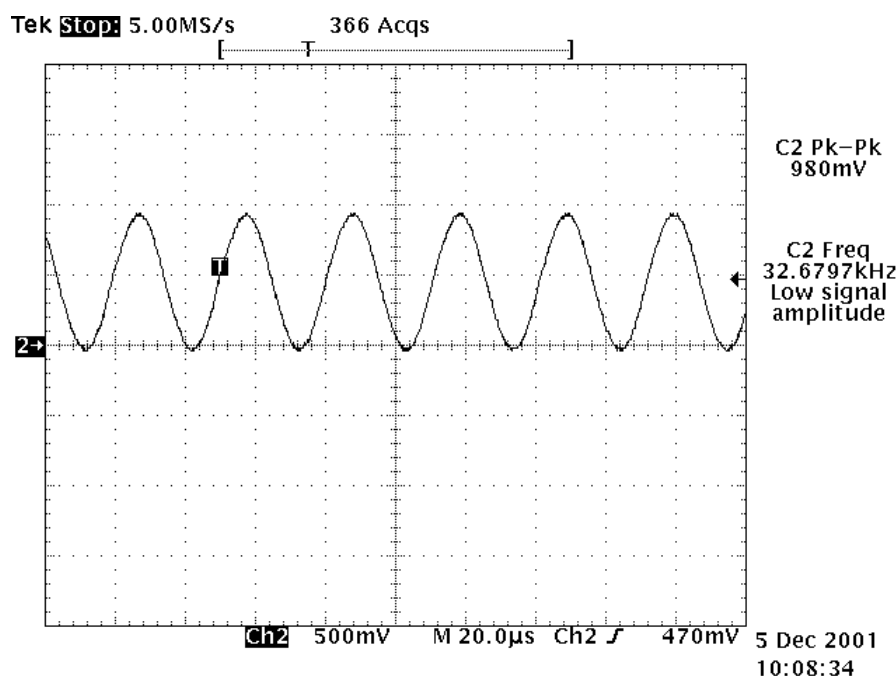


Figure 9: 32 KHz analog sleep clock signal

## Flash Programming

### Connections to Baseband

The flash programming equipment is connected to the baseband using test pads for galvanic connection. The test pads are allocated in such a way that they can be accessed when the phone is assembled. The flash programming interface consists of the VPP, FBUSTX, FBUSRX, MBUS, and BSI signals and is used by the FPS-8 to flash. The connection is through the UEM, which means that the logic voltage levels correspond to 2.78 V. Power is supplied to the phone using the battery contacts.

### Baseband Power Up

The baseband power is controlled by the flash prommer in production and in re-programming situations. Applying supply voltage to the battery terminals causes the baseband to power up. Once the baseband is powered, flash programming indication begins (see the following "Flash Programming Indication" section).

### Flash Programming Indication

Flash programming is indicated to the UPP using the MBUSRX signal between the UPP and UEM. The MBUS signal from the baseband to the flash prommer is used as a clock for the synchronous communication. The flash prommer keeps the MBUS line low during UPP boot to indicate that the flash prommer is connected. If the UPP MBUSRX signal is low on the UPP, the MCU enters flash-programming mode. In order to avoid accidental entry to the flash-programming mode, the MCU only waits for a specified time to get

input data from the flash prommer. If the timer expires without any data being received, the MCU continues the boot sequence. The MBUS signal from the UEM to the external connection is used as a clock during flash programming. This means that the flash-programming clock is supplied to the UPP on the MBUSRX signal.

The flash prommer indicates flash programming/reprogramming to the UEM by writing an 8-bit password to the UEM. The data is transmitted on the FBUSRX line and the UEM clocks the data on the FBUSRX line into a shift register. When the 8 bits have been shifted in the register, the flash prommer generates a falling edge on the BSI line. This loads the shift register content in the UEM into a compare register. Programming starts if the 8-bits in the compare register match with the default value preset in the UEM. At this point the flash prommer pulls the MBUS signal to UEM low in order to indicate to the MCU that the flash prommer is connected. The UEM reset state machine performs a reset to the system, PURX low for 20 ms. The UEM flash programming mode is valid until the MCU sets a bit in the UEM register that indicates the end of flash programming. Setting this bit also clears the compare register in the UEM, which was loaded at the falling edge of the BSI signal. The UEM watchdogs are disabled during the flash programming mode. Setting the bit indicating the end of flash programming enables and resets the UEM watchdog timer to its default value. Clearing the flash programming bit also causes the UEM to generate a reset to the UPP.

The BSI signal is used to load the value into the compare register. In order to avoid spurious loading of the register, the BSI signal is gated during the UEM master reset and during power on when PURX is active. The BSI signal should not change states during normal operation unless the battery is extracted. In this case the BSI signal will be pulled high. Note that a falling edge is required to load the compare register.

## Flashing

Flash programming is done through the VPP, FBUSTX, FBUSRX, MBUS, and BSI signals.

When the phone enters flash programming mode, the prommer indicates to the UEM that flash programming will take place by writing an 8-bit password to the UEM. A prommer first sets the BSI to "1", uses FBUSRX for writing, and uses the MBUS for clocking. The BSI is then set back to "0".

The MCU uses the FBUSTX signal to indicate to the prommer that it has been noticed. Then the MCU reports the UPP type ID and is ready to receive the secondary boot code in its internal SRAM.

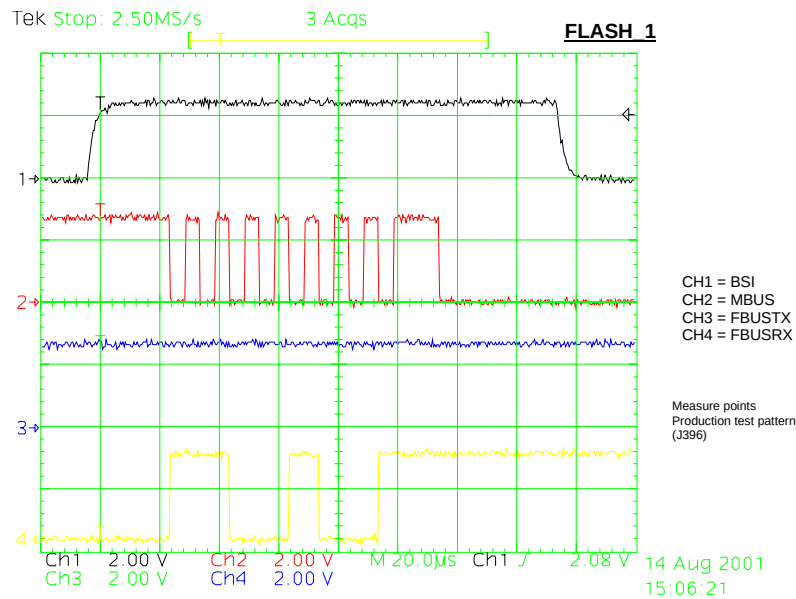


Figure 10: Flashing start

This boot code asks the MCU to report the prommer phone's configuration information, including the flash device type. Now the prommer can select and send the algorithm code to the MCU SRAM (and SRAM/Flash self-tests can be executed).

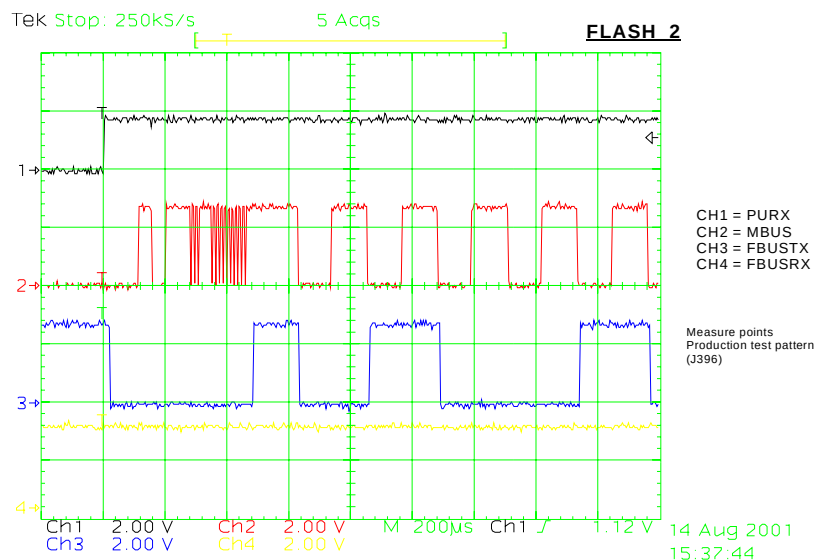


Figure 11: Flashing, continued 1

- Ch1-> PURX
- Ch2-> MBUS toggled three times for MCU initialization
- Ch3-> FBUS\_TX low, MCU indicates that prommer has been noticed
- Ch4-> FBUS\_RX

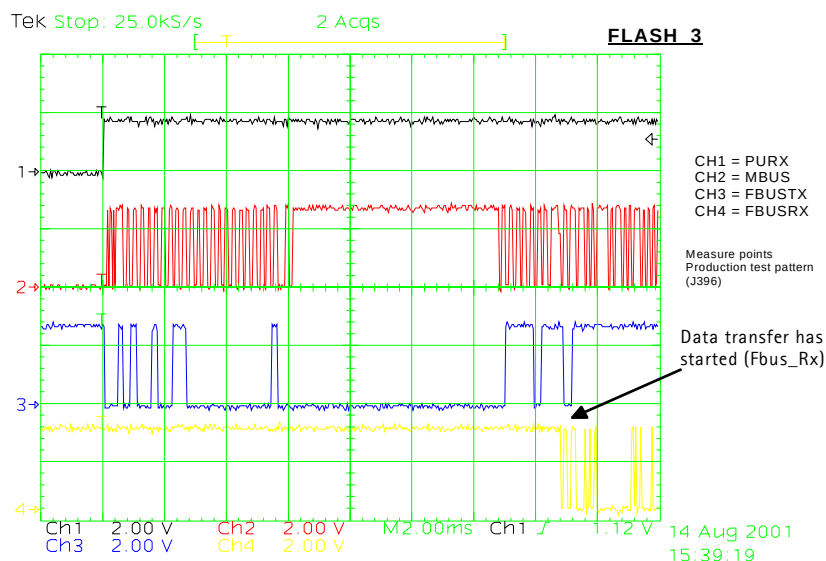


Figure 12: Flashing, continued 2

### Flash Programming Error Codes

The following characteristics apply to the information in Table 3.

- Error codes can be seen from the test results or from Phoenix's flash-tool.
- Underlined information means that the connection under consideration is being used for the first time.

Table 3: Flash programming error codes

| Error | Description                                                                                                                                                  | Not Working Properly                                                                                                                                                                                                                             |
|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| C101  | "The Phone does not set FbusTx line high after the startup."                                                                                                 | <u>Vflash1</u><br><u>VBatt</u><br><u>BSI and FbusRX from prommer to UEM.</u><br><u>FbusTx from UPP-&gt;UEM-&gt;Prommer(SA0)</u>                                                                                                                  |
| C102  | "The Phone does not set FbusTx line low after the line has been high. The Prommer generates this error also when the Phone is not connected to the Prommer." | <u>PURX(also to Safari)</u><br><u>VR3</u><br><u>Rfclock(VCTCX0-&gt;Safari-&gt;UPP)</u><br><u>Mbus from Prommer-&gt;UEM-&gt;UPP(MbusRx)(SA0)</u><br><u>FbusTx from UPP-&gt;UEM-&gt;Prommer(SA1)</u><br><u>BSI and FbusRX from prommer to UEM.</u> |
| C103  | " Boot serial line fail."                                                                                                                                    | <u>Mbus from Prommer-&gt;UEM-&gt;UPP(MbusRx)(SA1)</u><br><u>FbusRx from Prommer-&gt;UEM-&gt;UPP</u><br><u>FbusTx from UPP-&gt;UEM-&gt;Prommer</u>                                                                                                |
| C104  | "MCU ID message sending failed in the Phone."                                                                                                                | <u>FbusTx from UPP-&gt;UEM-&gt;Prommer</u>                                                                                                                                                                                                       |
| C105  | "The Phone has not received Secondary boot codes length bytes correctly."                                                                                    | <u>Mbus from Prommer-&gt;UEM-&gt;UPP(MbusRx)</u><br><u>FbusRx from Prommer-&gt;UEM-&gt;UPP</u><br><u>FbusTx from UPP-&gt;UEM-&gt;Prommer</u>                                                                                                     |

Table 3: Flash programming error codes (Continued)

| Error                | Description                                                                                                                       | Not Working Properly                                                                                  |
|----------------------|-----------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------|
| C106                 | "The Phone has not received Secondary code bytes correctly."                                                                      | Mbus from Prommer->UEM->UPP(MbusRx)<br>FbusRx from Prommer->UEM->UPP<br>FbusTx from UPP->UEM->Prommer |
| C107                 | "The Phone MCU can not start Secondary code correctly."                                                                           | UPP                                                                                                   |
| C586                 | "The erasing status response from the Phone informs about fail."                                                                  | Flash                                                                                                 |
| C686                 | "The programming status response from the Phone informs about fail."                                                              | Flash                                                                                                 |
| Cx81                 | "The Prommer has detected a checksum error in the message, which it has received from the Phone."                                 | FbusTx from UPP->UEM->Prommer                                                                         |
| Cx82                 | "The Prommer has detected a wrong ID byte in the message, which it has received from the Phone."                                  | FbusTx from UPP->UEM->Prommer                                                                         |
| A204                 | "The flash manufacturer and device IDs in the existing algorithm files do not match with the IDs received from the target phone." | Flash<br>UPP<br>VIO/VANA<br>Signals between UPP-Flash                                                 |
| Cx83                 | "The Prommer has not received phone acknowledge to the message."                                                                  | Mbus from Prommer->UEM->UPP(MbusRx)<br>FbusRx from Prommer->UEM->UPP<br>FbusTx from UPP->UEM->Prommer |
| Cx84                 | "The phone has generated NAK signal during data block transfer."                                                                  |                                                                                                       |
| Cx85                 | "Data block handling timeout"                                                                                                     |                                                                                                       |
| Cx87                 | "Wrong MCU ID."                                                                                                                   | RFclock<br>UPP(Vcore)                                                                                 |
| Startup for flashing | Required startup for flashing                                                                                                     | Vflash1<br>VBatt                                                                                      |

## Charging Operation

### Battery

The RM-11 uses a Lithium-Ion cell battery (BLD-3) with a capacity of 780 mAh. Reading a resistor inside the battery pack on the BSI line indicates the battery size. An NTC resistor inside the battery measures the battery temperature on the BTEMP line.

Temperature and capacity information are needed for charge control. These resistors are connected to BSI and BTEMP pins of the battery connector. The phone has 100 kW pull-up resistors for these lines so that they can be read by A/D inputs in the phone.

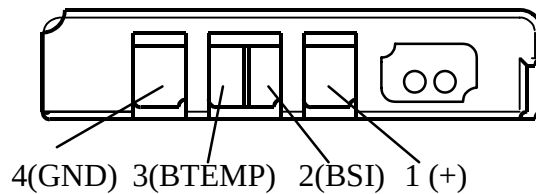


Figure 13: BLD-3 battery pack pin order

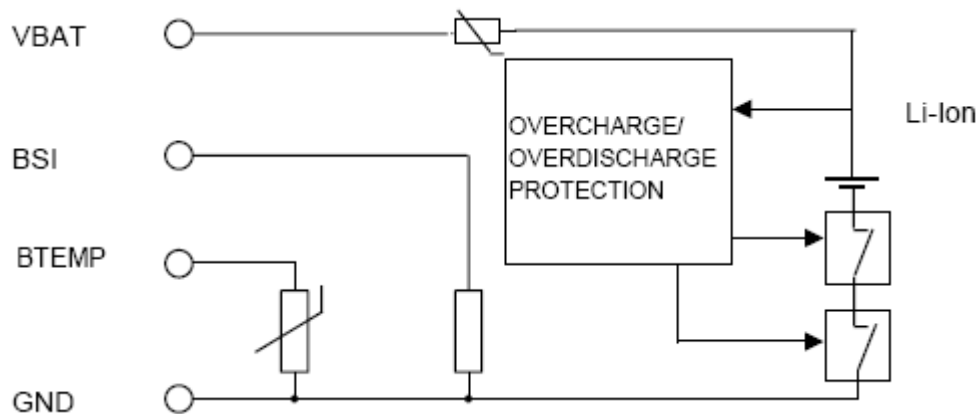


Figure 14: Interconnection diagram inside the battery pack

### Charging Circuitry

The UEM ASIC controls charging depending on the charger being used and the battery size. External components are needed for EMC, reverse polarity and transient protection of the input to the baseband module. The charger connection is through the system connector interface. The RM-11 baseband is designed to support DCT3 chargers from an electrical point of view. Both two-wire and three-wire type chargers are supported. However, 3-wire chargers are treated as 2-wire chargers.

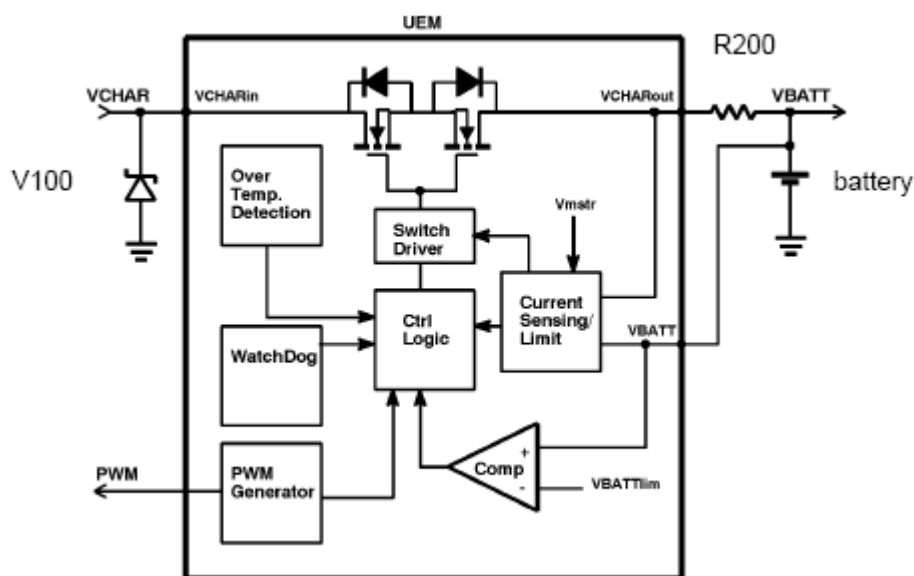


Figure 15: Charging circuitry

## Charger Detection

Connecting a charger creates voltage on the VCHAR input of the UEM. Charging starts when the UEM detects that the VCHAR input voltage level is above 2 V (VCHdet+ threshold). The VCHARDET signal is generated to indicate the presence of the charger for the SW. The charger identification/acceptance is controlled by EM SW.

The charger recognition is initiated when the EM SW receives a "charger connected" interrupt. The algorithm basically consists of the following three steps:

1. Check that the charger output (voltage and current) is within safety limits.
2. Identify the charger as a two-wire or three-wire charger.
3. Check that the charger is within the charger window (voltage and current).

If the charger is accepted and identified, the appropriate charging algorithm is initiated.

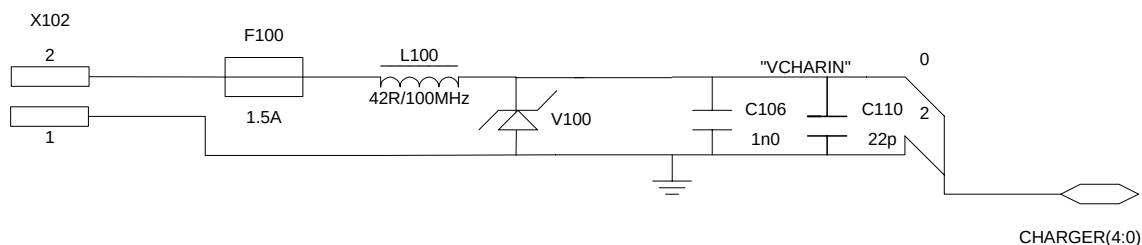


Figure 16: Charging circuit

## Charge Control

In active mode, charging is controlled by the UEM's digital part. Charging voltage and current monitoring is used to limit charging into a safe area. For that reason, the UEM has the following programmable, charging cut-off limits:

- VBATLim1=3.6 V (Default)
- VBATLim2L=5.0 V
- VBATLim2H=5.25 V

VBATLim1, 2L, 2H are designed with hystereses. When the voltage rises above VBATLim1, 2L, 2H+ charging is stopped by turning the charging switch off. There is no change in the operational mode. Charging restarts after the voltage decreases below VBATLim-.

There are two PWM frequencies in use depending on the type of the charger. A two-wire charger uses a 1 Hz, and a three-wire charger uses a 32 Hz. The duty cycle range is 0% to 100%, and the maximum charging current is limited to 1.2 A.

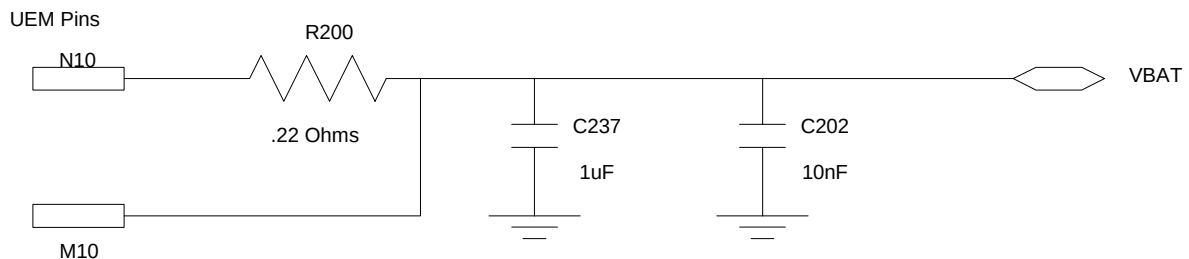


Figure 17: Charging circuit at battery

## Audio

The audio control and processing in RM-11 is supported by the UEM and the UPP. The UEM contains the audio codec. The UPP contains the MCU and DSP blocks, handling and processing the audio data signals.

The baseband supports three microphone inputs and two earpiece outputs. The microphone inputs are:

- MIC1 = Used for the phone's internal microphone
- MIC2 = Used for headsets (HDB-4)
- MIC3 = Used for the Universal Headset

Every microphone input can have either a differential or single-ended AC connection to the UEM circuit. In RM-11, the internal microphone (MIC1) and external microphone (MIC2) are both differential for Tomahawk accessory detection. However, the Universal Headset interface is single-ended. The microphone signals from different sources are connected to separate inputs at the UEM. Inputs for the microphone signals are differential types. Also, the MICB1 is used for MIC1, and MICB2 is used for both MIC2 and MIC3 (Universal Headset).

## Display and Keyboard

The RM-11 uses LEDs for LCD and keypad illumination. There are three LEDs for the LCD and eight LEDs for the keypad. The KLIGHT signal is used to drive the LED driver for the LCD and keyboard.

The RM-11 also uses a color LCD. The interface utilizes a 9-bit data transfer and is similar to the DCT3-type interface, except the Command/Data information is transferred together with the data.

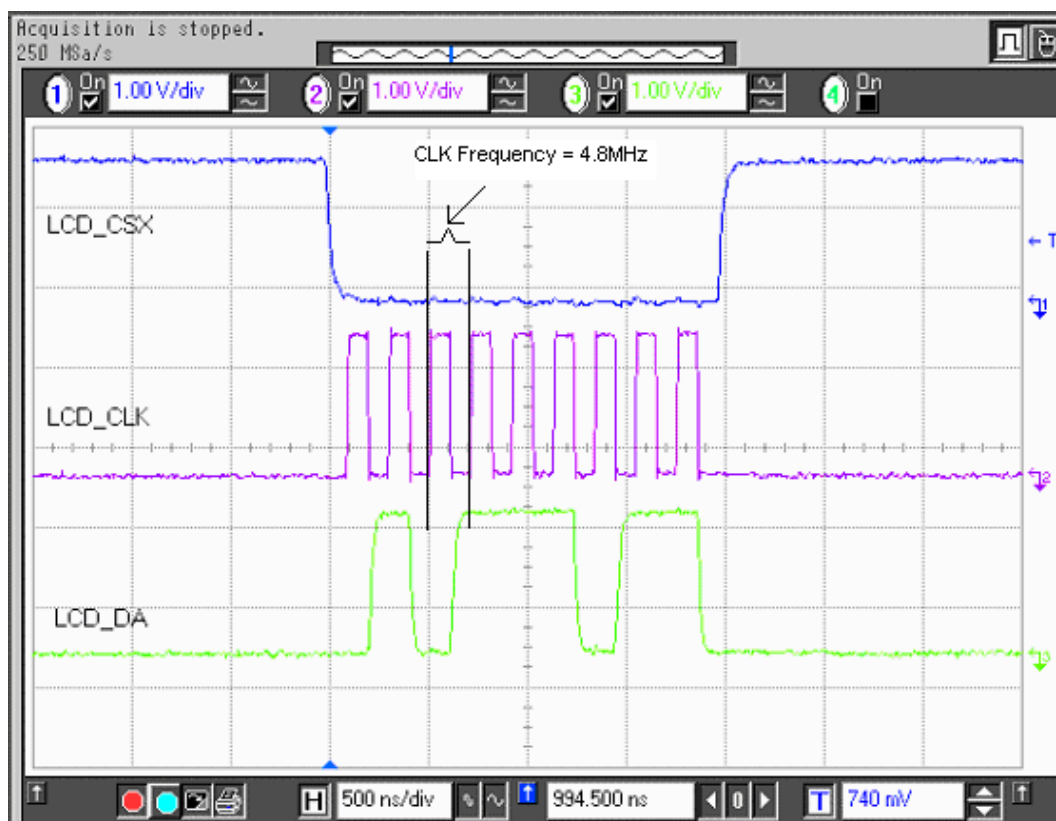


Figure 18: D/C bit set during each transmitted byte

## Flashlight

The flashlight feature on C-Rio is driven by the White LED Driver and controlled by the UEM. The circuit for the flashlight is driven by TK11851TL. In this situation, the driver is used as a boost DC/DC.  $V_{out}$  is set using three precision resistors in R300, R316, and 317.  $V_{out} = V_{fb} * (1 + (R316 + R317) / R300)$ . The TK11851L is an active-high enable device, whose enable signal is tied to Klight/Dlight signals from the UEM. When Klight goes high it turns on the TK11851TL driver and the V301 transistor, which allows a path to GND.

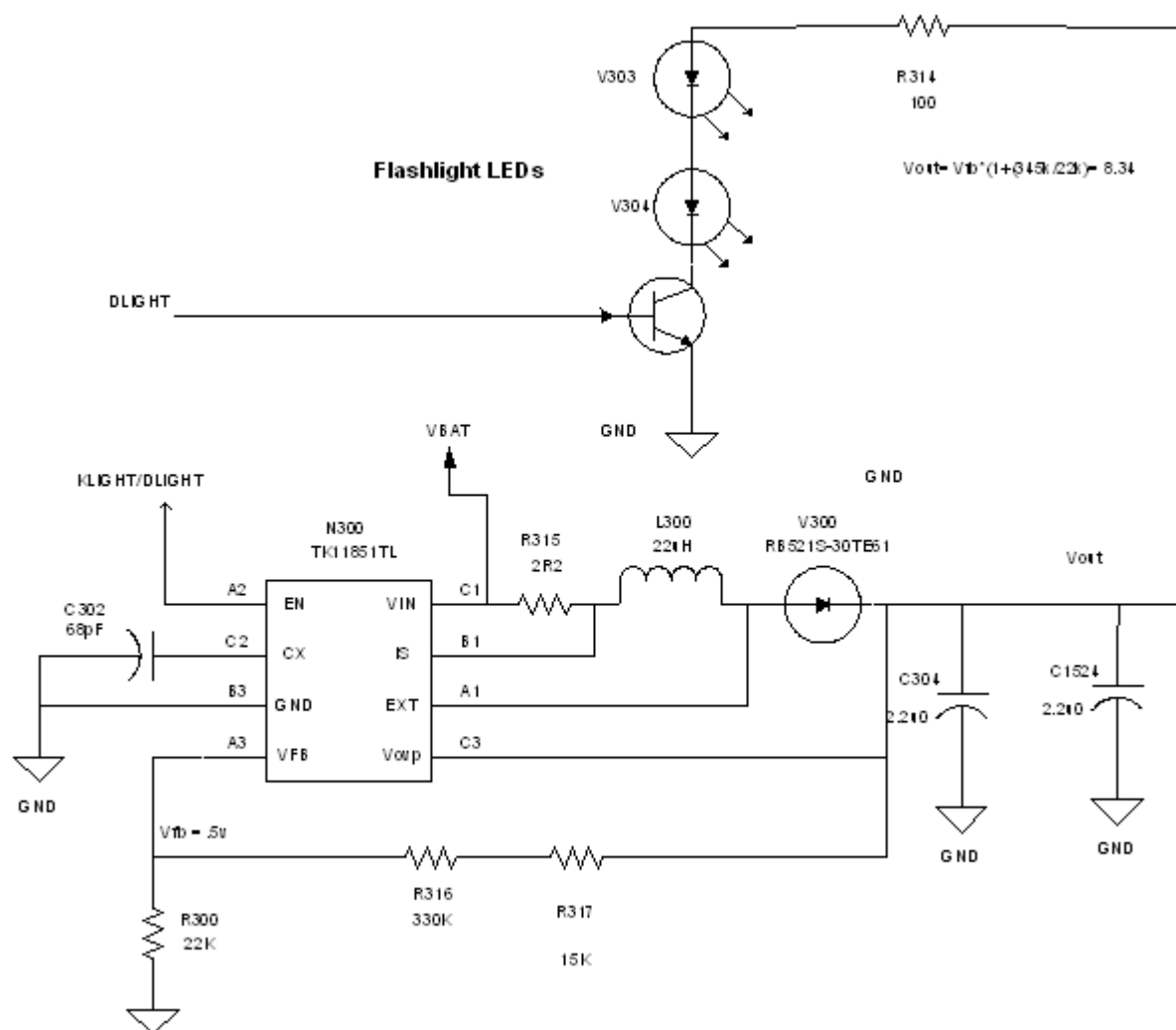


Figure 19: Circuit for the flashlight being driven by TK11851TL

## Camera

This section describes the tests of the camera module part of baseband. All the other tests are described in the *C-Rio BaseBand Test Specification* document.

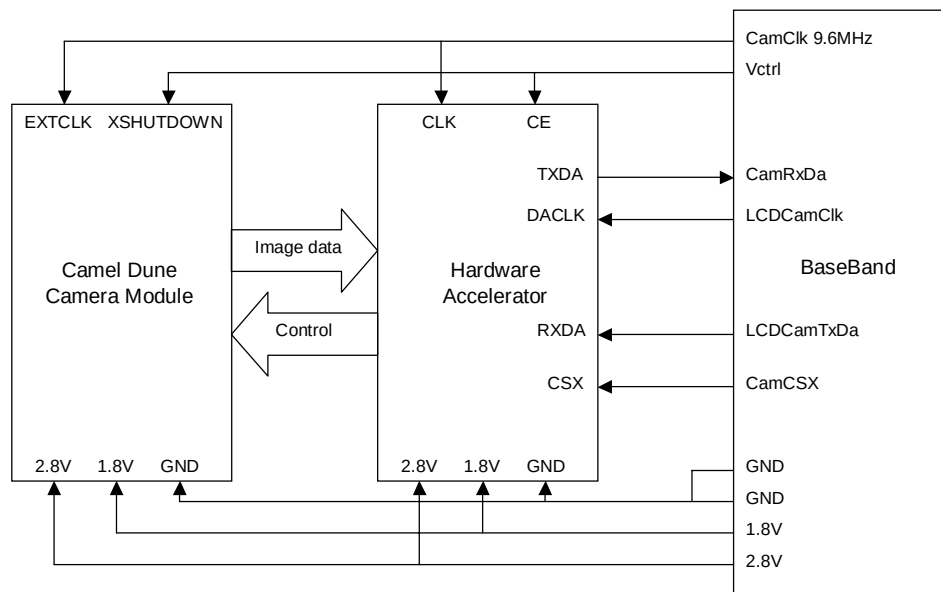


Figure 20: Camera and HWA connections to the baseband

## DC Measurements

Table 4: Power supply characteristics

| Signal name    | Measured value (V) | Min | Typical | Max | Unit | Description    |
|----------------|--------------------|-----|---------|-----|------|----------------|
| VIO            | 1.8                | 1.7 | 1.8     | 1.9 | V    | Control line   |
| VANA (Vflash2) | 2.79               | 2.7 | 2.78    | 2.9 | V    | Analog supply  |
| VDIG           | 1.79               | 1.7 | 1.8     | 1.9 | V    | Digital supply |
| GND            | 0                  |     | 0       |     | V    | System GND     |

Table 5: DC characteristics

| Signal name | Measured value (V)   | Min                | Typical | Max                  | Unit | Description                                     |
|-------------|----------------------|--------------------|---------|----------------------|------|-------------------------------------------------|
| CSX         | H = 1.80<br>L = 2.0m | H: 0.7xVIO<br>L: 0 |         | H: VIO<br>L: 0.3xVIO | V    | Camera chip-select (active low)                 |
| DaClk       | H = 1.77<br>L = -18m | H: 0.7xVIO<br>L: 0 |         | H: VIO<br>L: 0.3xVIO | V    | Voltage levels                                  |
| TxDa        | H = 1.75<br>L = -18m | H: 0.8xVIO<br>L: 0 |         | H: VIO<br>L: 0.2xVIO | V    | Data to transmit, camera interrupt (active low) |

Table 5: DC characteristics (Continued)

| Signal name | Measured value (V)   | Min                | Typical | Max                  | Unit | Description       |
|-------------|----------------------|--------------------|---------|----------------------|------|-------------------|
| RxDa        | H = 1.76<br>L = -11m | H: 0.7xVIO<br>L: 0 |         | H: VIO<br>L: 0.3xVIO | V    | Data to receive   |
| ExtClk      | H = 1.75<br>L = -12m | 0.5Vp-p            | 1Vp-p   | VIOp-p               | V    | All modes         |
| VCtrl       | N/A                  | H: 0.7xVIO<br>L: 0 |         | H: VIO<br>L: 0.3xVIO | V    | Logic 0: shutdown |

Note: H indicates high signal level and L indicates low signal level.

## AC Measurements

Table 6: AC characteristics

| Signal name | Measured value (V) | Min   | Typical | Max   | Unit | Description                    |
|-------------|--------------------|-------|---------|-------|------|--------------------------------|
| DaCLK       | F = 4.799          | 4.69  | 4.8     | 4.81  | MHz  | Frequency                      |
|             | D = 49.4           | 45/55 | 50/50   | 55/45 | %    | Duty cycle                     |
| ExtClk      | F = 9.6            | 9.59  | 9.6     | 9.69  | MHz  | External system clock (mode 4) |
|             | D = 49.3           | 45/55 | 50/50   | 45/55 | %    |                                |

Note: DaClk frequency will not exceed ExtClk/2.

## Timing Measurements

### Signal Descriptions

The chip-select CSX enables and disables the camera serial bus. The CSX is active low. An additional function of CSX during the power-up sequence is to determine the communication mode of the HWA (UIF or CCI/CCP).

DaClk is a serial data clock and is typically set to ExtClk/2. The clock can be driven low when data is not transmitted, but may be running when the CSX is inactive as well.

RxDa data length is 8 bits + D/C-bit. The first bit to be received is a D/C-bit, which indicates to the camera the status of the following 8 bit data. The D/C-bit is low ('0') in the case of command data to the camera. The camera must not react to the received data if the D/C-bit is high ('1').

TxDa data length is 8 bits + TxEnd-bit. The first bit to be transmitted is the TxEnd-bit, which indicates if the data is the last byte from the image frame. When a byte is the last byte of an image frame from the camera, the TxEnd-bit is set high ('1'). Otherwise the

TxEnd-bit is set low ('0') by the camera. The camera can interrupt the baseband by driving TxDa low for at least one ExtClk cycle when not transferring an image. The interrupt is initiated by the falling edge of the signal.

ExtClk is the external system clock for the camera module. The clock may be AC or DC coupled. Four fixed frequencies are available (8.4, 9.6, 9.72, 13, and 16.8 MHz, each within  $\pm 100\text{kHz}$ ).

VIO is a regulated 1.8 V nominal I/O logic supply for the camera module.

VCtrl is a control signal to place the camera and HWA in their lowest power consumption modes. It must be permissible to pull this signal up if this functionality is not required.

VANA is a regulated 2.78 V nominal voltage from the engine to the camera module.

GND is system GND for the camera module.

### Power-up Timing

The purpose of this test is to measure the power-up timing.

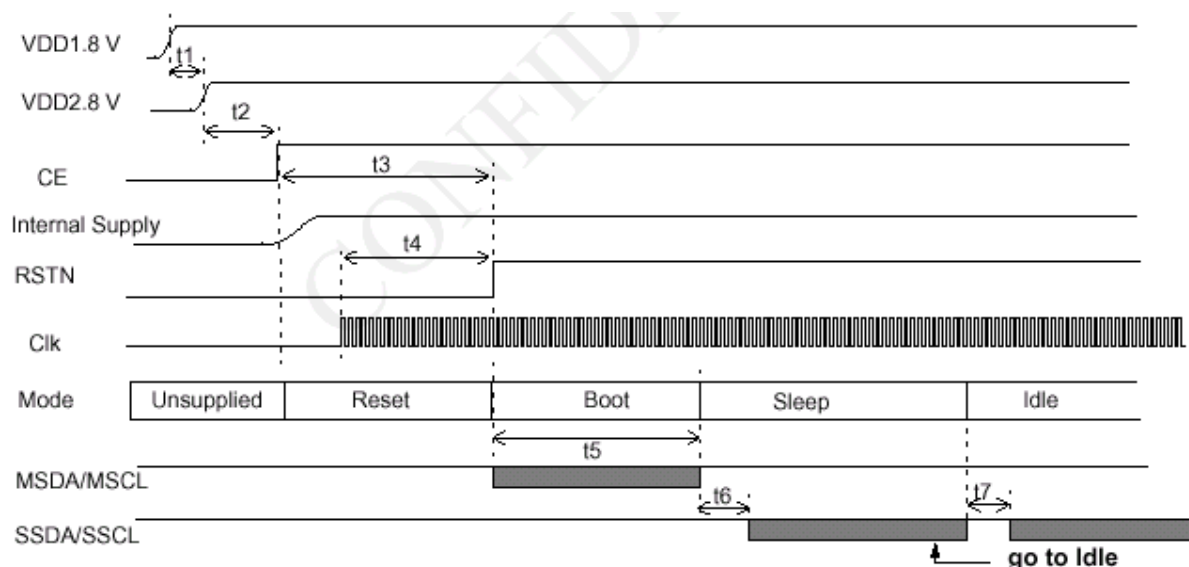


Figure 21: Power-up timing

Table 7 includes the test parameters for power-up timing

Table 7: Power-up timing

| Parameter | Measured value | Limit  | Notes                     |
|-----------|----------------|--------|---------------------------|
| t1        | N/A            | >0     |                           |
| t2        | 68us           | >0     |                           |
| t3        | 134us@1.3v     | >120us | Determined by external RC |
| t4        | 119.5us@1.3v   | >100us |                           |

Table 7: Power-up timing (Continued)

| Parameter | Measured value | Limit | Notes                          |
|-----------|----------------|-------|--------------------------------|
| t5        | 3.75ms         | >5ms  | Software dependent             |
| t6        | N/A            | >0    | SSDA and SSCL signals not used |
| t7        | N/A            | >8ms  | SSDA and SSCL signals not used |

### UIF Interface Timing Measurements

The purpose of this test is to measure the timing of UIF serial interface. The rise and fall times are also measured.

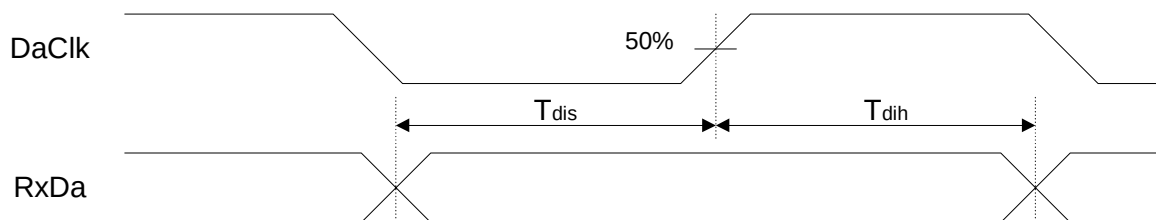


Figure 22: Timing diagram of DaClk and RxDa signals

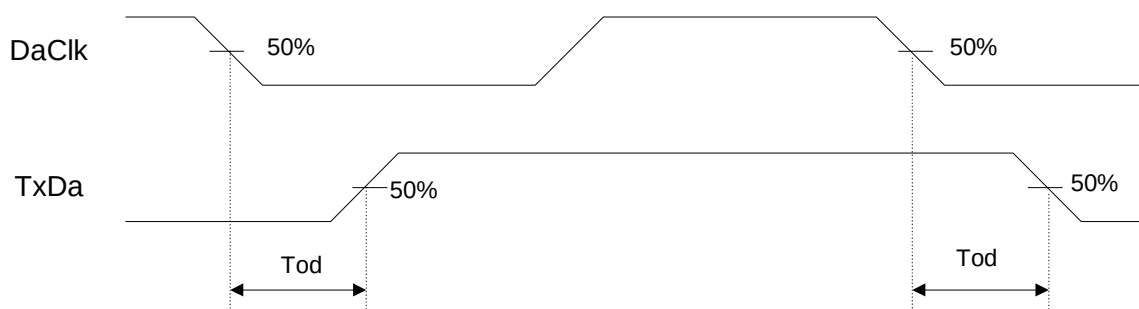


Figure 23: Timing diagram of DaClk and TxDa signals

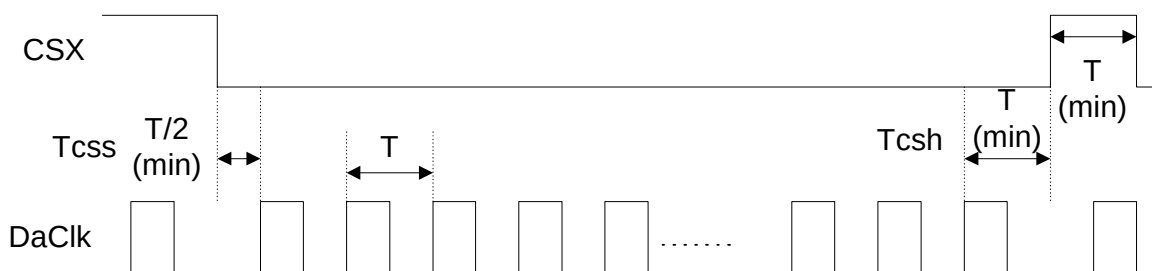


Figure 24: Timing diagram of CSX and DaClk signals

Table 8: Timing margins of serial interface for camera module

| Parameter                          | Measured Value | Min Time             | Max Time |
|------------------------------------|----------------|----------------------|----------|
| RxDa data set-up time (Tdis)       | 100ns          | 25ns                 |          |
| RxDa data hold time (TdiH)         | 103.6ns        | 25ns                 |          |
| CSX valid to DaClk high (Tcss)     | 106ns          | (DaClk cycle time)/2 |          |
| DaClk high to CSX invalid (Tcsh)   | 209ns          | DaClk cycle time     |          |
| Camera interrupt (TxDa pin) (Tint) | 204ns          | 1 x ExtClk cycle     |          |
| Output delay time (C=30pF) (Tod)   | 8.3ns          |                      | 20ns     |

Figure 25 shows the rise and fall times of the serial interface and limits shown in Table 9.

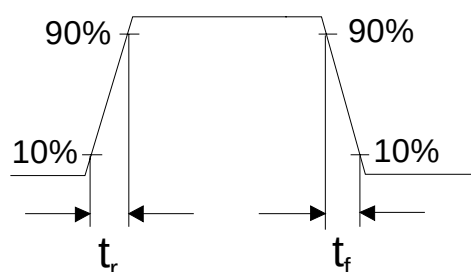


Figure 25: Rise and fall times

Table 9 shows the rise and fall times for each parameter.

Table 9: Rise and fall times of serial interface for camera module

| Parameter       | Measured Value | Min Time | Max Time |
|-----------------|----------------|----------|----------|
| RxDa rise time  | 8.63ns         |          | 20ns     |
| RxDa fall time  | 4.79ns         |          | 20ns     |
| CSX rise time   | 8.41ns         |          | 20ns     |
| CSX fall time   | 4.76ns         |          | 20ns     |
| TxDa rise time  | 3.21ns         | 10ns     | 30ns     |
| TxDa fall time  | 2.84ns         | 10ns     | 30ns     |
| DaClk rise time | 6.31ns         |          | 20ns     |
| DaClk fall time | 4.47ns         |          | 20ns     |

## FM Radio

FM radio circuitry is implemented using a highly integrated radio IC (TEA5767HN). The MCU SW controls FM radio circuitry through a serial bus (GenIOS) interface.

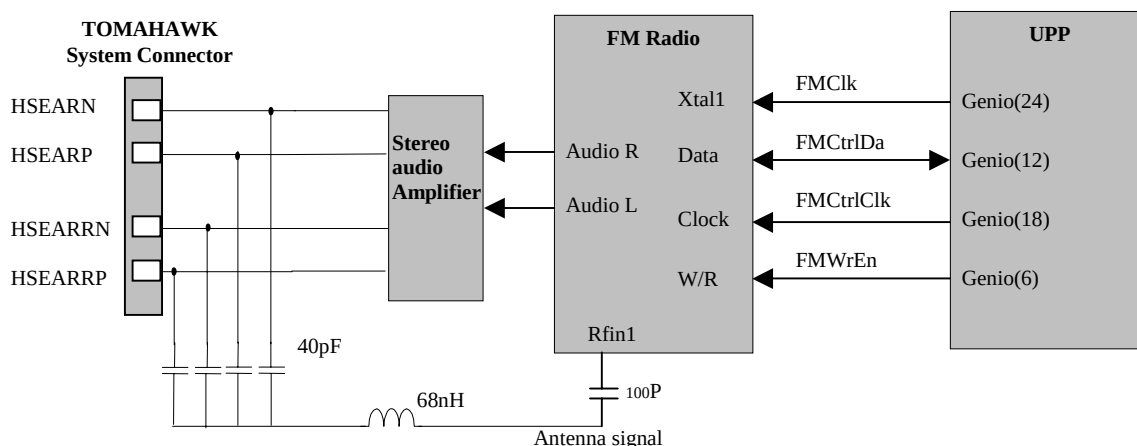


Figure 26: FM Radio (N356) Audio (N150)-, antenna- and digital interface connections

Table 10 shows the FM radio interface timing for the FMWrEn, FMCtrlClk, and FMCtrlDa radio signals.

Table 10: FM radio interface timing

| FM Radio Signal | Min                      | Nom | Max   | Condition                                            | Notes                                                                                                                                                                                                                                        |
|-----------------|--------------------------|-----|-------|------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| FMWrEn          | 20μs                     |     |       | $t_{wd}$                                             | FMWrEn high before rising edge of FMCtrlClk (write operation)                                                                                                                                                                                |
| FMCtrlClk       | 50ms                     |     | 1 μs  | $t_r/t_f$<br>$t_{start}$                             | Rise/fall time<br>FMCtrlClk delay after switching on the VFLASH2                                                                                                                                                                             |
| FMCtrlDa        | 10 μs<br>1.5 μs<br>20 μs |     | 14 μs | $t_{da}$<br>$t_{shift}$<br>$t_{hold}$<br>$t_{setup}$ | Shift register available after "search ready"<br>Data available after FMCtrlClk rising edge (read operation)<br>FMCtrlDa stable after FMCtrlClk rising edge (write operation)<br>FMCtrlDa set before FMCtrlClk rising edge (write operation) |

While the WRITE/READ is HIGH, the microcontroller can transmit data to the TEA5767. At the rising edge of the Bus clock, the register shifts and accepts the stable bit. At clock LOW the micro controller writes the following bit. A tuning function is started when the WRITE/READ signal changes from HIGH to LOW. If a search tuning request was sent, the IC autonomously starts searching the FM band. The search direction and search stop level can be chosen. If a station with a field strength equal to or higher than this stop

level is found, the tuning system stops and the Found Flag bit is set to HIGH. If a band limit was reached during the search, the tuning system stops at the band limit, the Band Limit flag bit is set to HIGH, and the Found Flag is set to HIGH.

While the WRITE/READ is LOW, data can be read by the UPP. At the rising edge of the BUS Clock, data will be shifted out of the register. This data is available from the point where the bus clock is HIGH until the next rising edge of the clock occurs.

The stereo audio output signal is fed to the stereo amplifier. Volume control of the FM audio signal is made by circuitry inside the amplifier. An amplified audio signal is fed to the headset or IHF speaker. The headset is also used as an antenna input for the radio.

### FM Radio Test

To hear the FM radio, first connect a headset to the Tomahawk or UHJ ports because the headset will be an FM radio antenna. Then, connect the headset to a UHJ port to control the FM radio by using Phoenix. If you connect a headset (such as HDS-3) to the Tomahawk connector, you can not control the phone because you have already occupied the connection port (Tomahawk). In this case you have to have jumper wires on production test points (Fbus Tx/RX,GND).

### Input Signals to FM Radio

After connecting a headset to the UHJ port to control the phone through Phoenix, you can see signals by turning on the FM radio in Phoenix. The FM radio menu is under the RF menu in Phoenix.

- FMClk — Test Point (FM04) : 32 KHz/1.8 V
- FMWrEn — Test Point (FM03) : Write enable at 1.8 V
- FMCtrlClk — Test Point (FM02) : Control clock at 1.8 V
- FMCtrlDa — Test Point (FM01) : Control data at 1.8 V

### FM Radio Signals **Before** Radio On

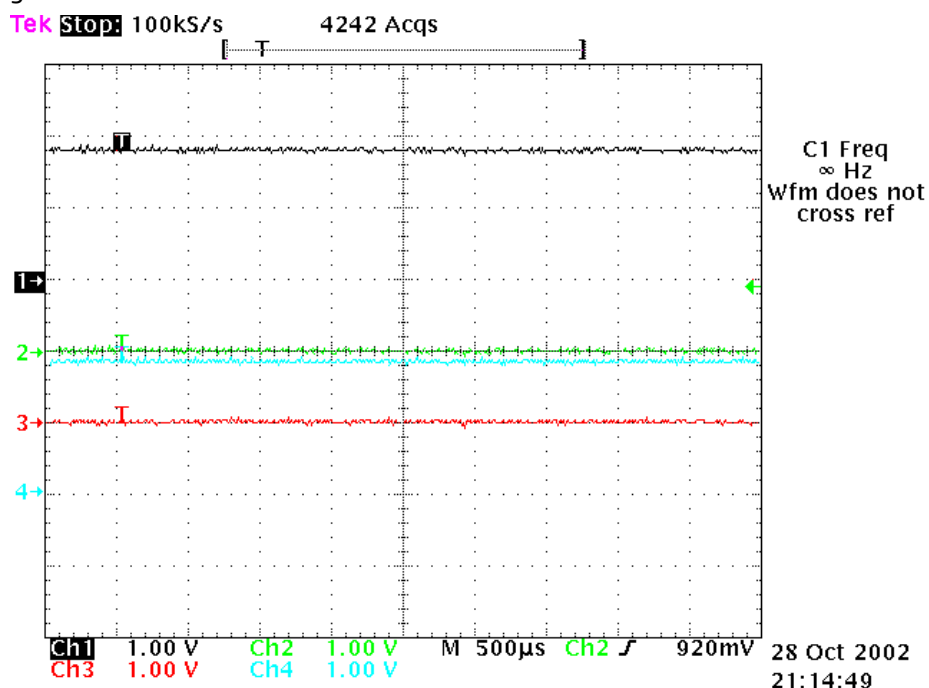


Figure 27: Ch1 : FMClk(32.768KHz) , Ch2 : FMWrEn, Ch3 : FMetriClk, Ch4 : FMetriDA

### FM Radio Signals **After** Radio On

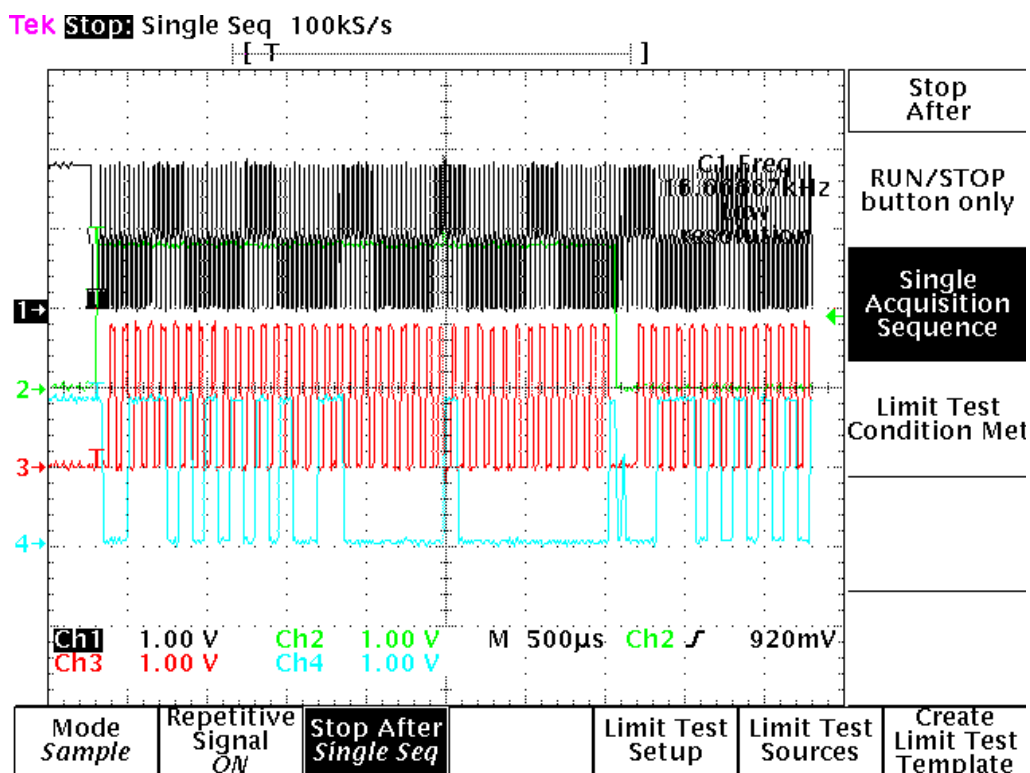


Figure 28: Radio signals after radio on

## Accessories

The RM-11 is designed to support Tomahawk and Universal Headset accessories, differential and single-ended, respectively. Detection of Tomahawk accessories is done through the ACI signal where the Universal Headset is detected on GenIO (21).

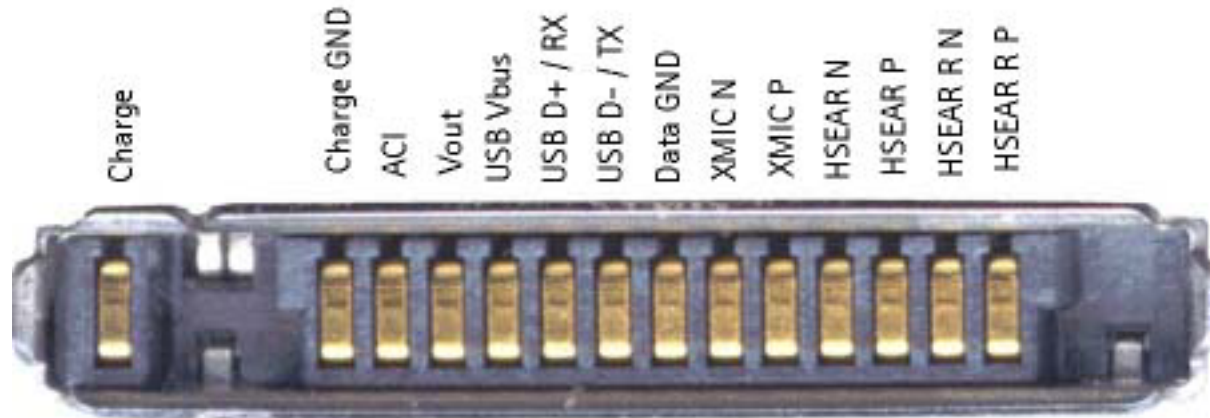


Figure 29: Pin out of the Tomahawk connector

You can perform the following functions in Tomahawk accessories:

- Charging
- Accessory detection
- FBUS communication
- USB communication
- Fully differential audio interface for mono and stereo outputs

These modes are explained in the following sections.

### Charging

Charging through Tomahawk is done the same way as through the charger connector. Pin 1 of the Tomahawk is physically connected the charger connector. When the phone is connected to the desktop charger (e.g., DCV-15) it is charged the same way as is done on the charger connector.

The actual charging sequence can be seen in Figure 30. The channels in the figure are as follows:

- CH1 = Charging current across the .22 Ohm (R200) resistor on UEMK
- CH2 = Charger voltage measure at V100
- CH3 = Battery voltage measure at R200
- CH4 = PURX

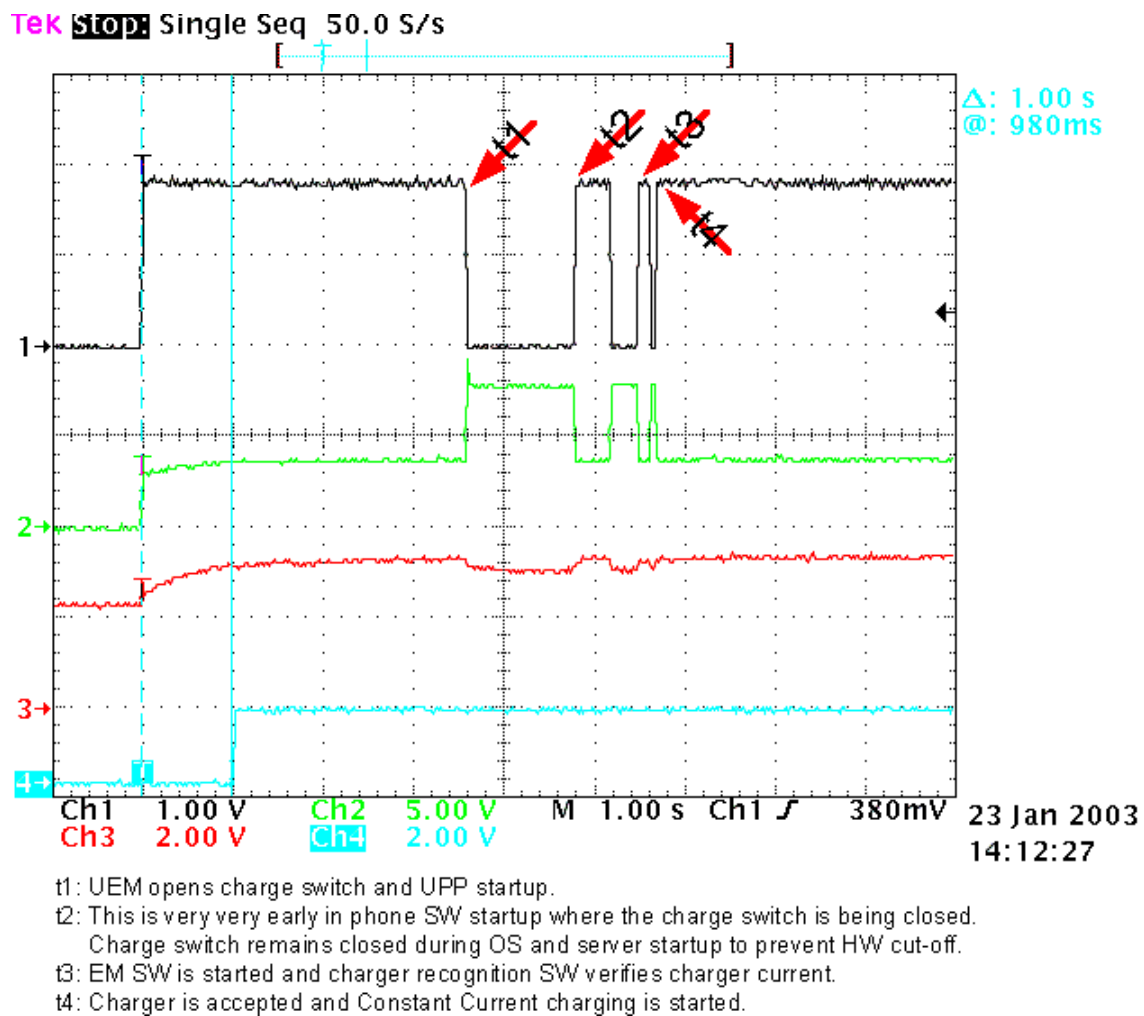


**Figure 30: Charging sequence**

Notice in Channel 4 that PURX is released. This is when the phone operation goes from RESET mode to POWER\_ON mode.

### Tomahawk Headset Detection

Accessory detection in Tomahawk is done digitally. The pins used for accessory detection are as follows:

- Pin 2 (Charge GND)
- Pin 3 (ACI)
- Pin 4 (Vout)

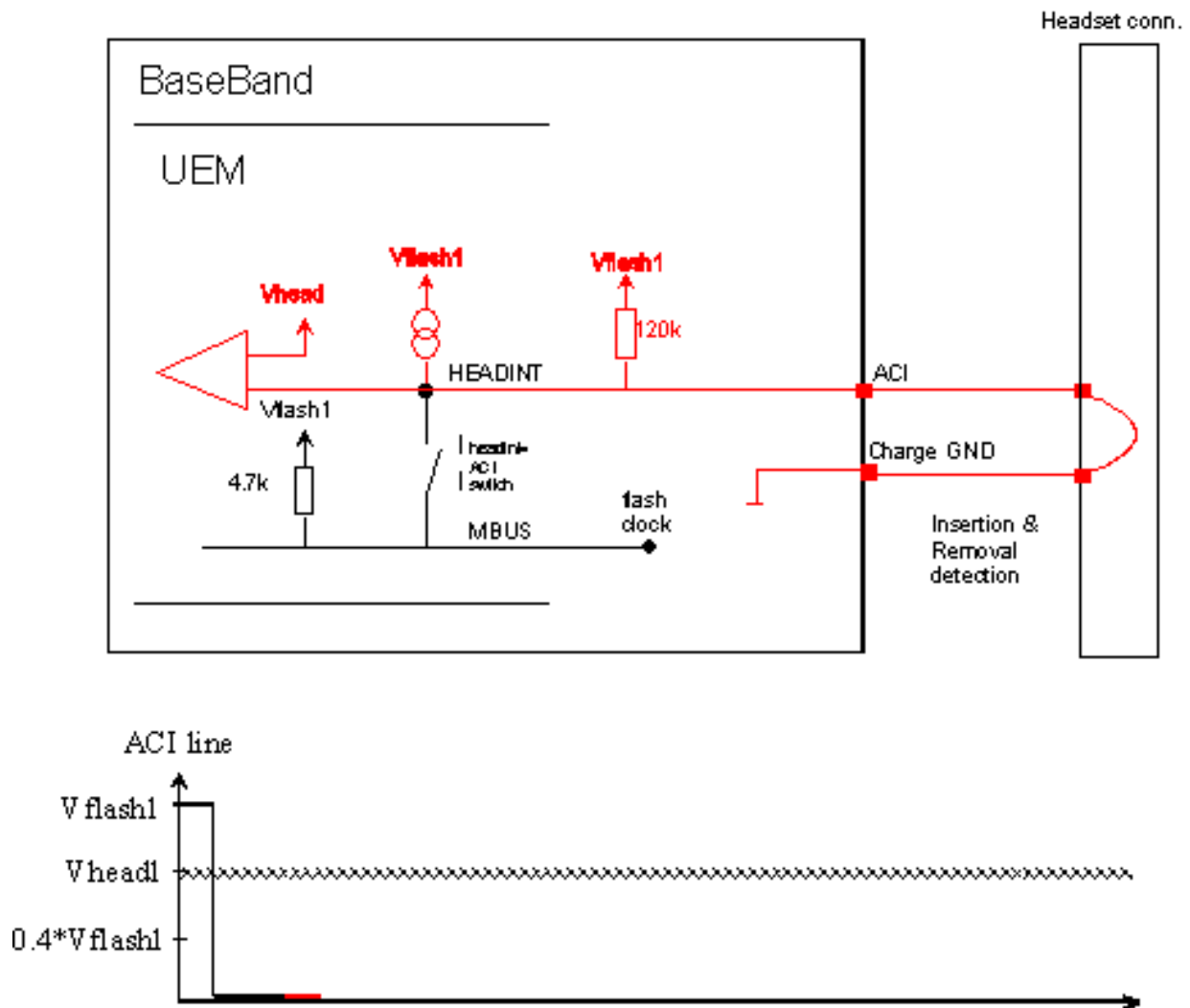


**Figure 31: A waveform of digital accessory detection**

## FBus Detection

FBus communication in Tomahawk is done through the following lines:

- Pin 2 (Charge GND)
- Pin 3 (ACI)
- Pin 4 (Vout)
- Pin 6 (FBus Rx)
- Pin 7 (FBus Tx)

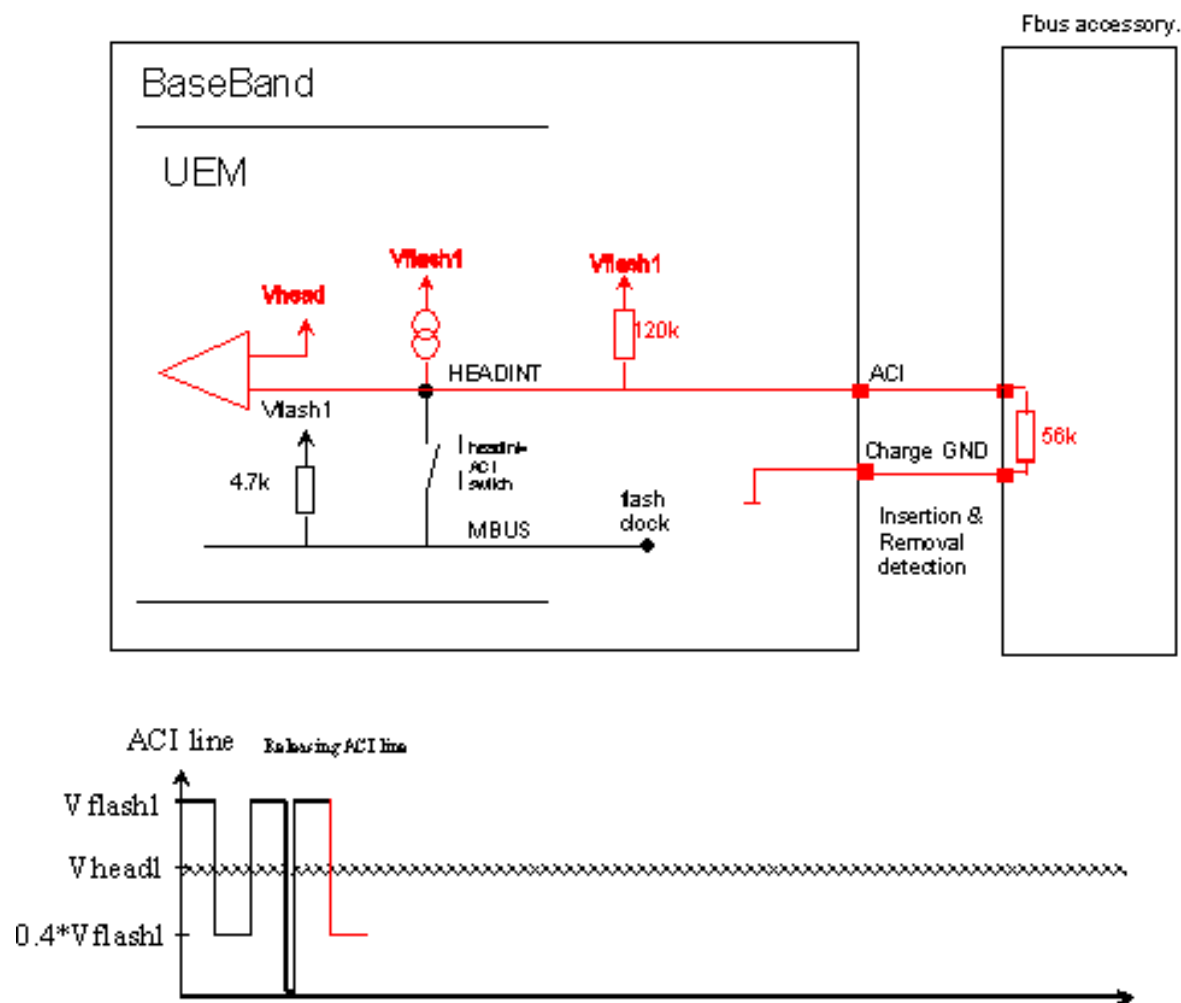


Figure 32: FBus communication in Tomahawk

### Accessory Detection Though ACI

USB and Audio on (mono or stereo) and FM radio communication in Tomahawk are done through the following signals:

Table 11: Accessory detection signals

| USB              | Audio/FM           |
|------------------|--------------------|
| Pin 5 (USB Vbus) | Pin 9 (XMic N)     |
| Pin 6 (USB +)    | Pin 10 (SMIC P)    |
| Pin 7 (USB -)    | Pin 11 (HSEAR N)   |
| Pin 8 (Data GND) | Pin 12 (HSEAR P)   |
|                  | Pin 13 (HSEAR R N) |
|                  | Pin 14 (HSEAR R P) |

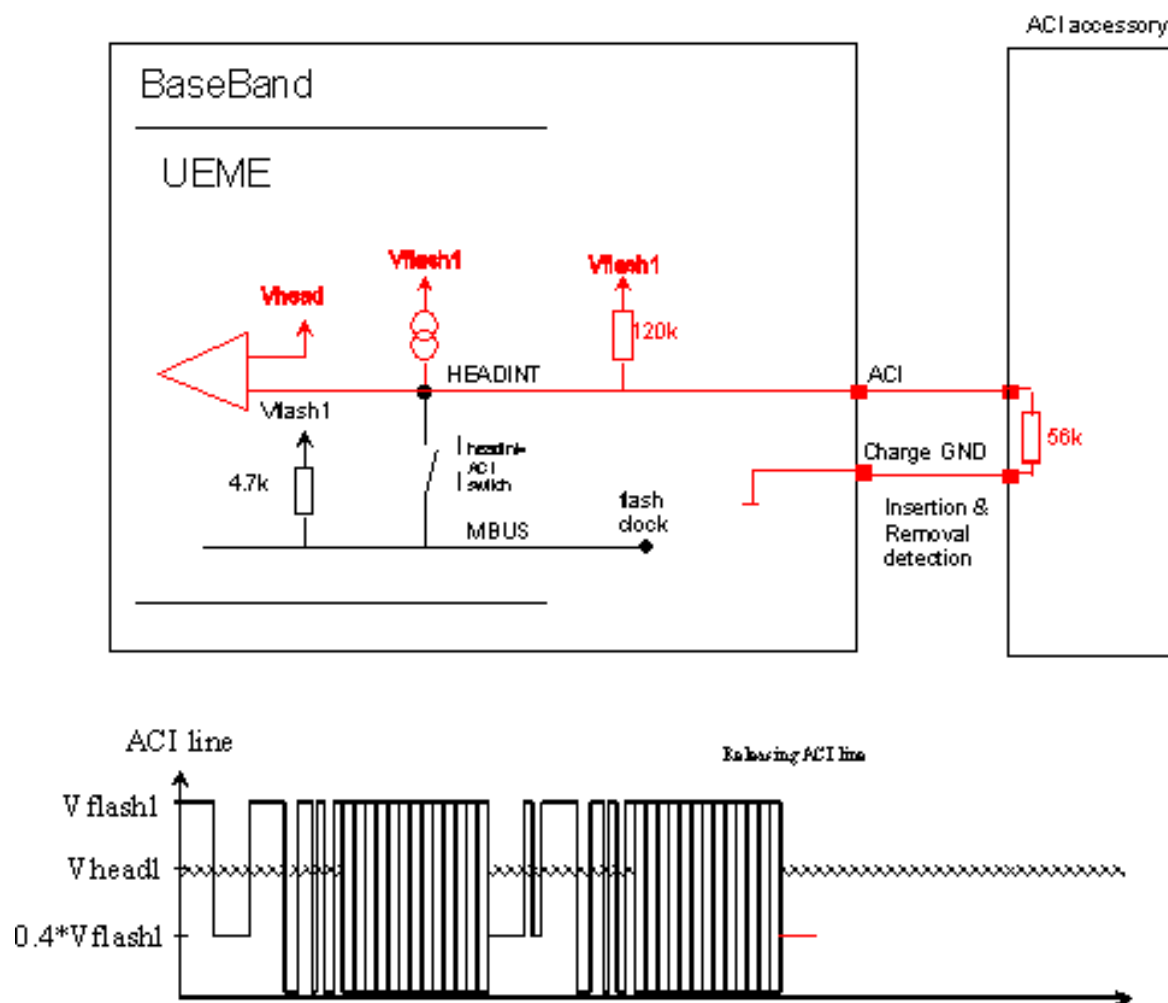


Figure 33: USB and Audio on (mono or stereo) and FM radio communication in Tomahawk

## RUIM (SIM CAR)

RM-11 supports RUIM for China products. The following waveform can be used to verify that sim\_vcc, sim\_i/o, sim\_clk, and sim\_rst signals are activated in the correct sequence at power up. This picture can be taken when the RUIM is installed on the phone and measures the signals when the phone is turned on. Figure 34 shows the proper waveforms when the interface is working. See Figure 36 on page 40 for the test point locations.

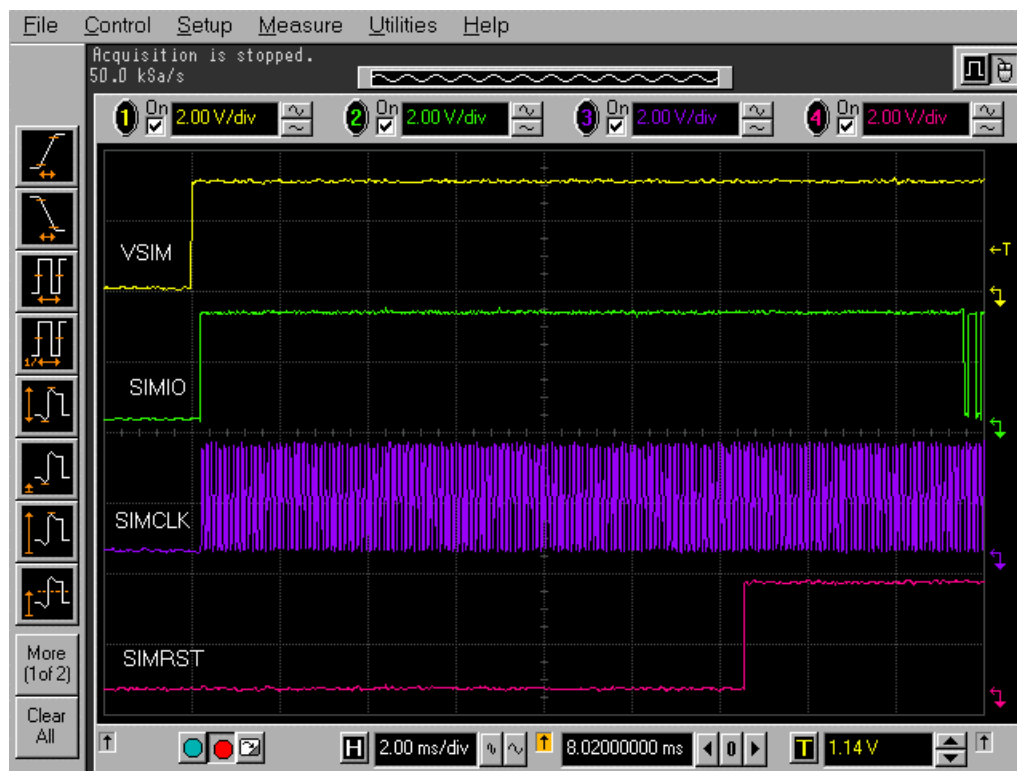


Figure 34: RUIM signal waveform

## Test Points

RM-11 BB test points, regulators, and BB ASICs.

Top View

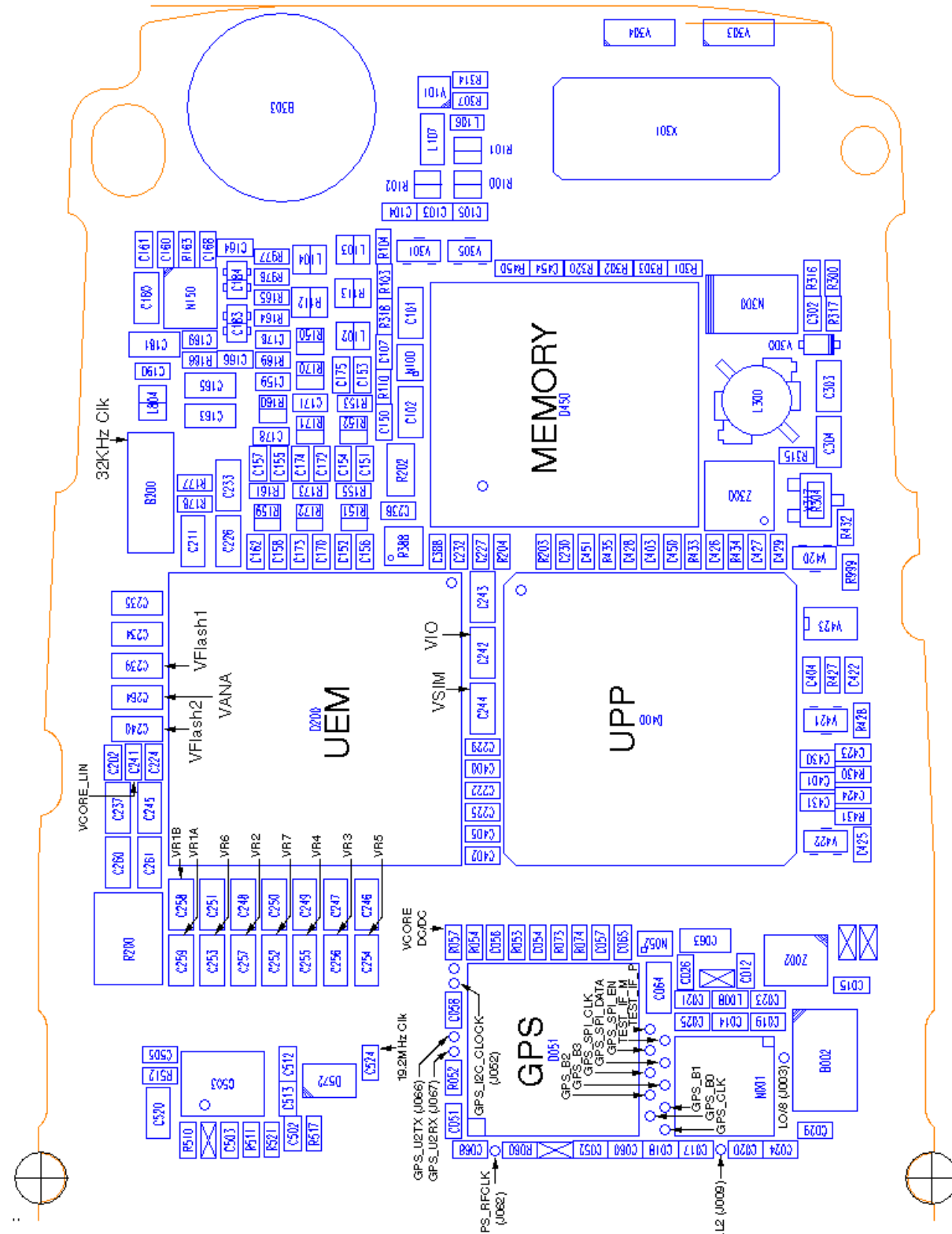


**Figure 35: Top view**

### Bottom View

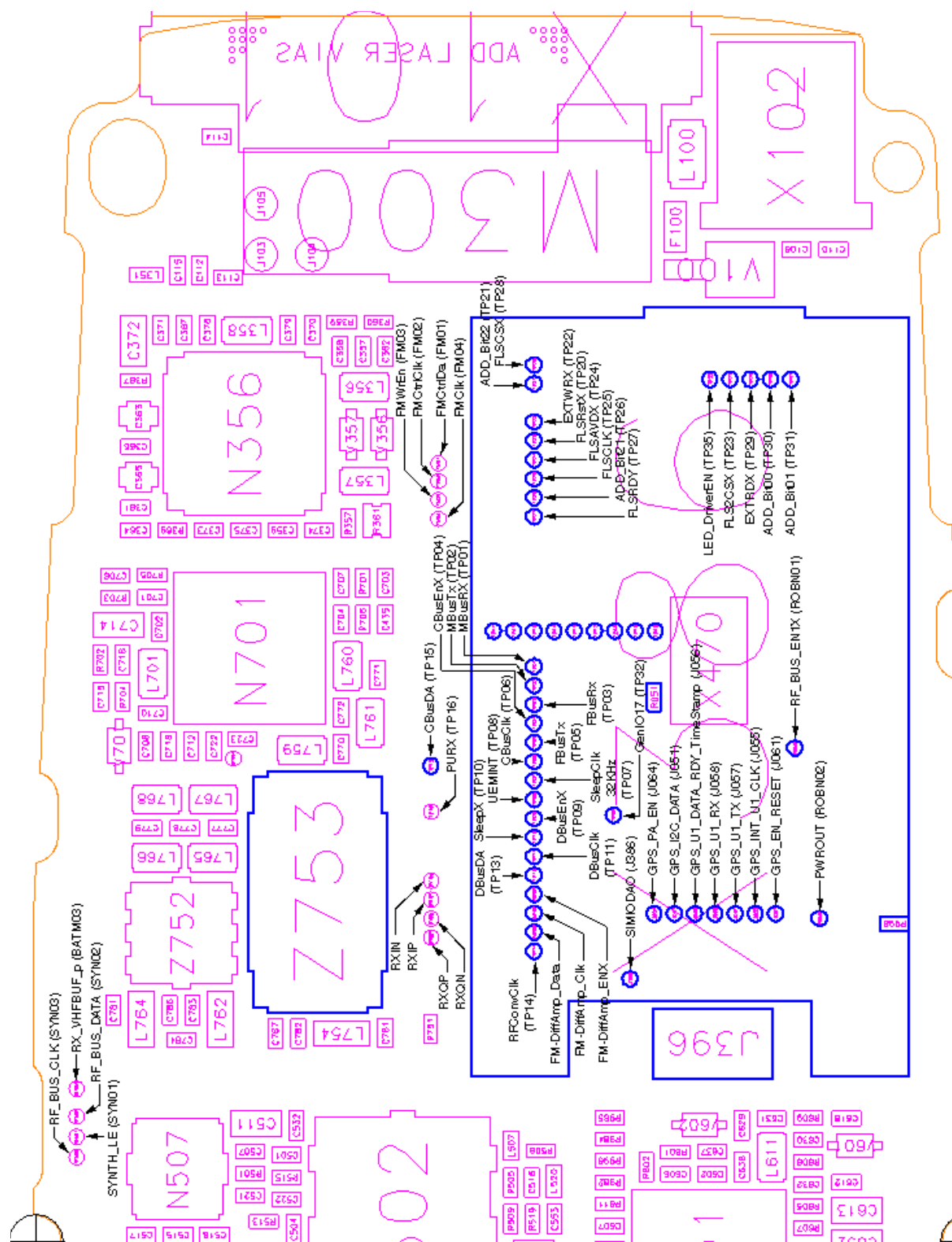


**Figure 36: Bottom view**

## Camera Test Points

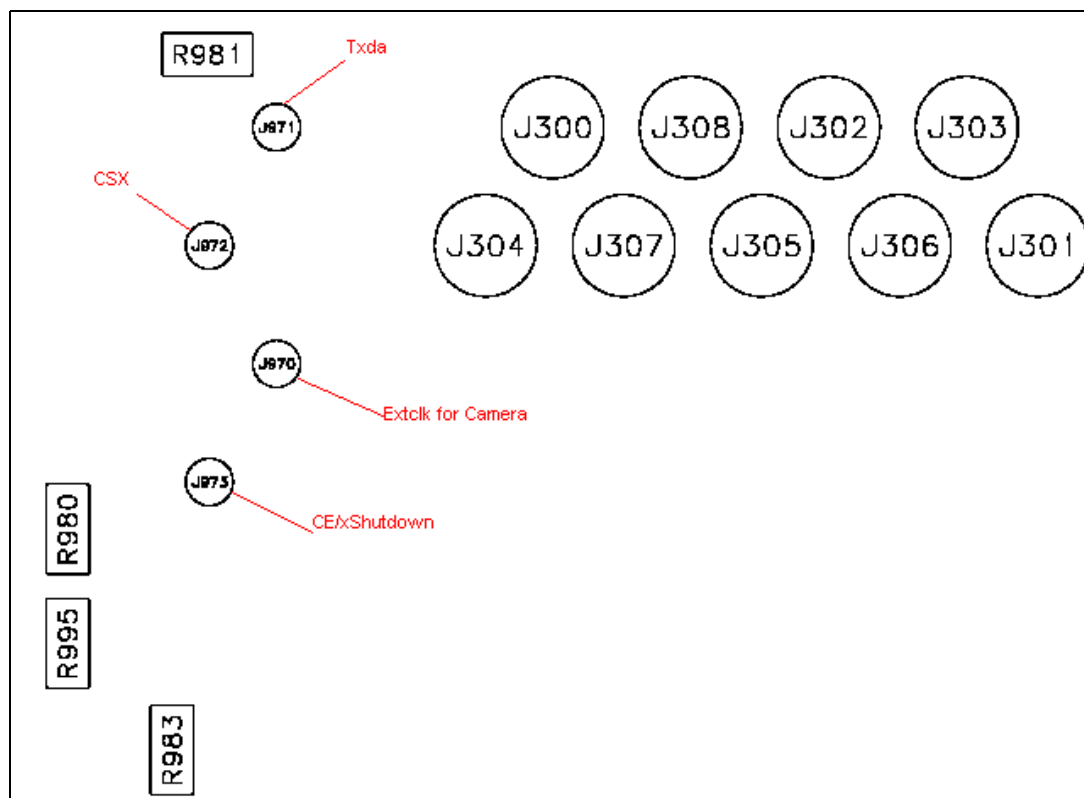
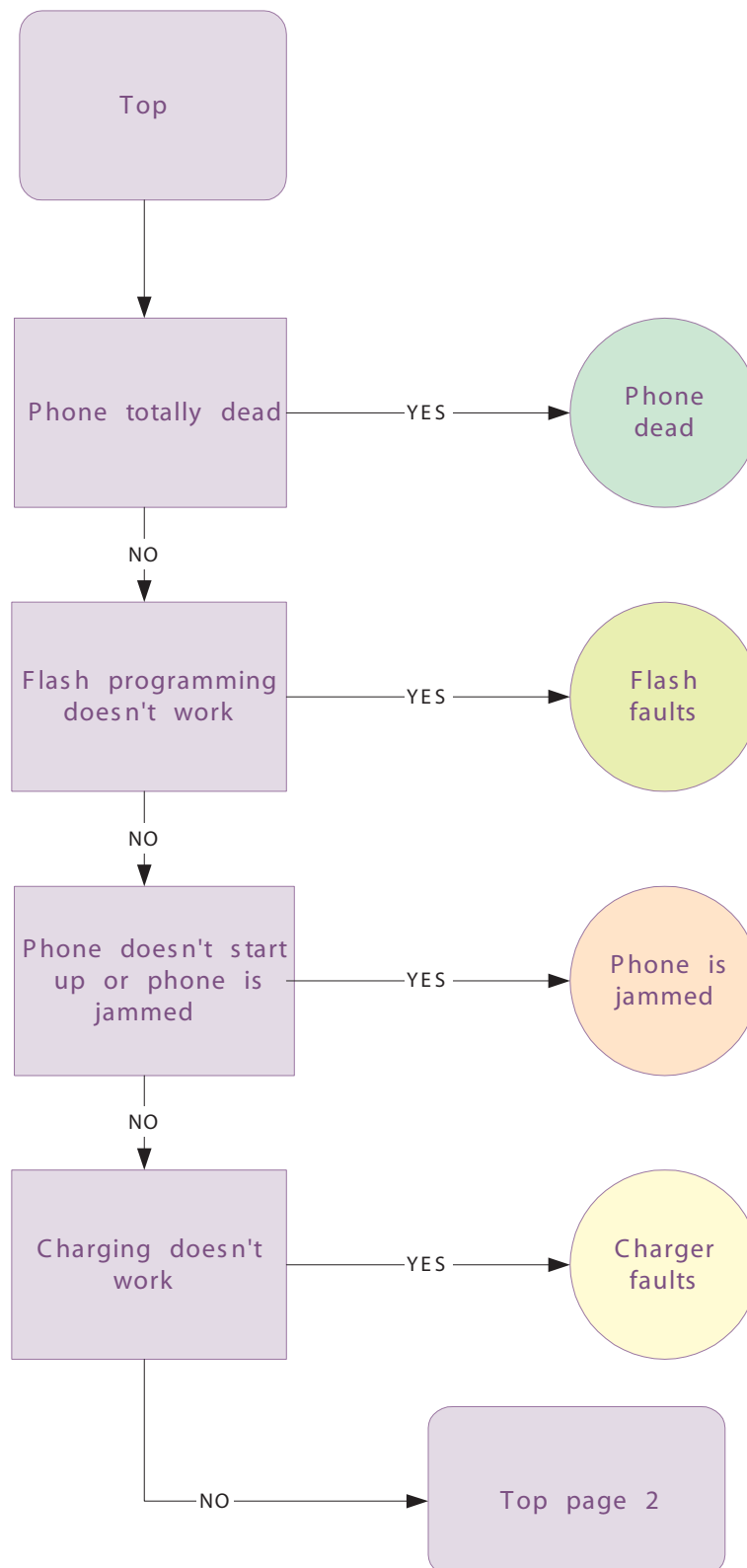
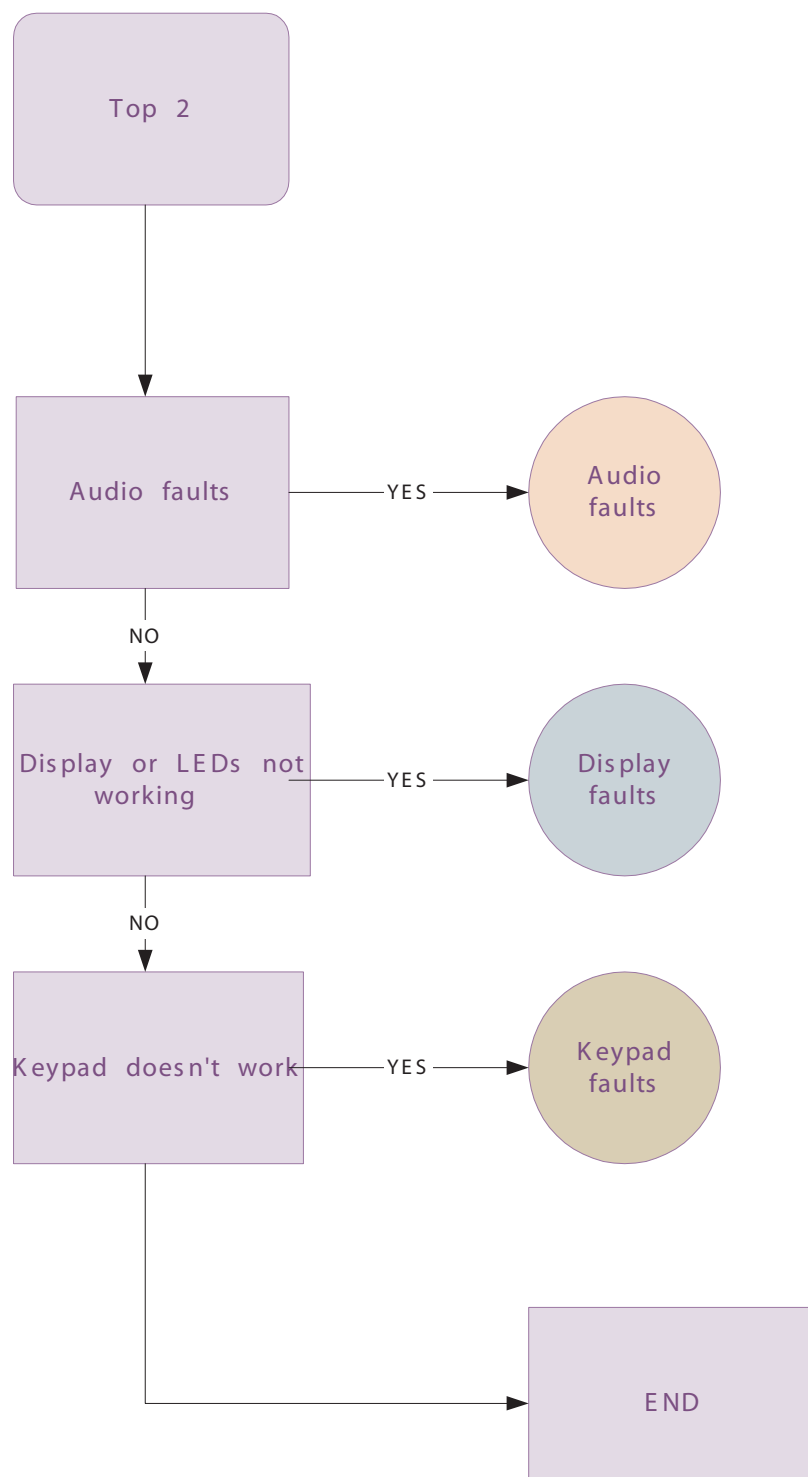


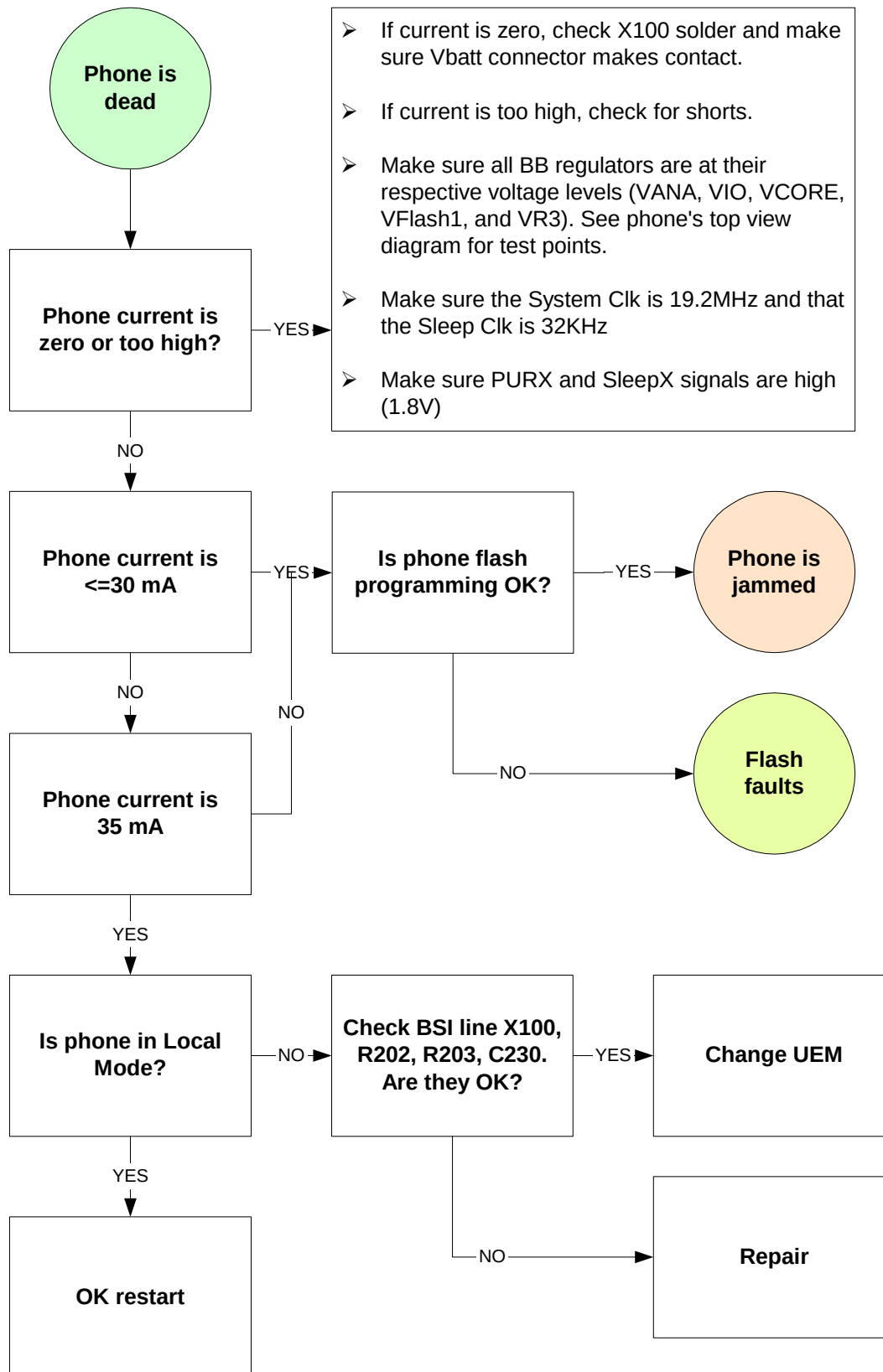
Figure 37: Camera test points; top side under LCD module

## Top Troubleshooting Map

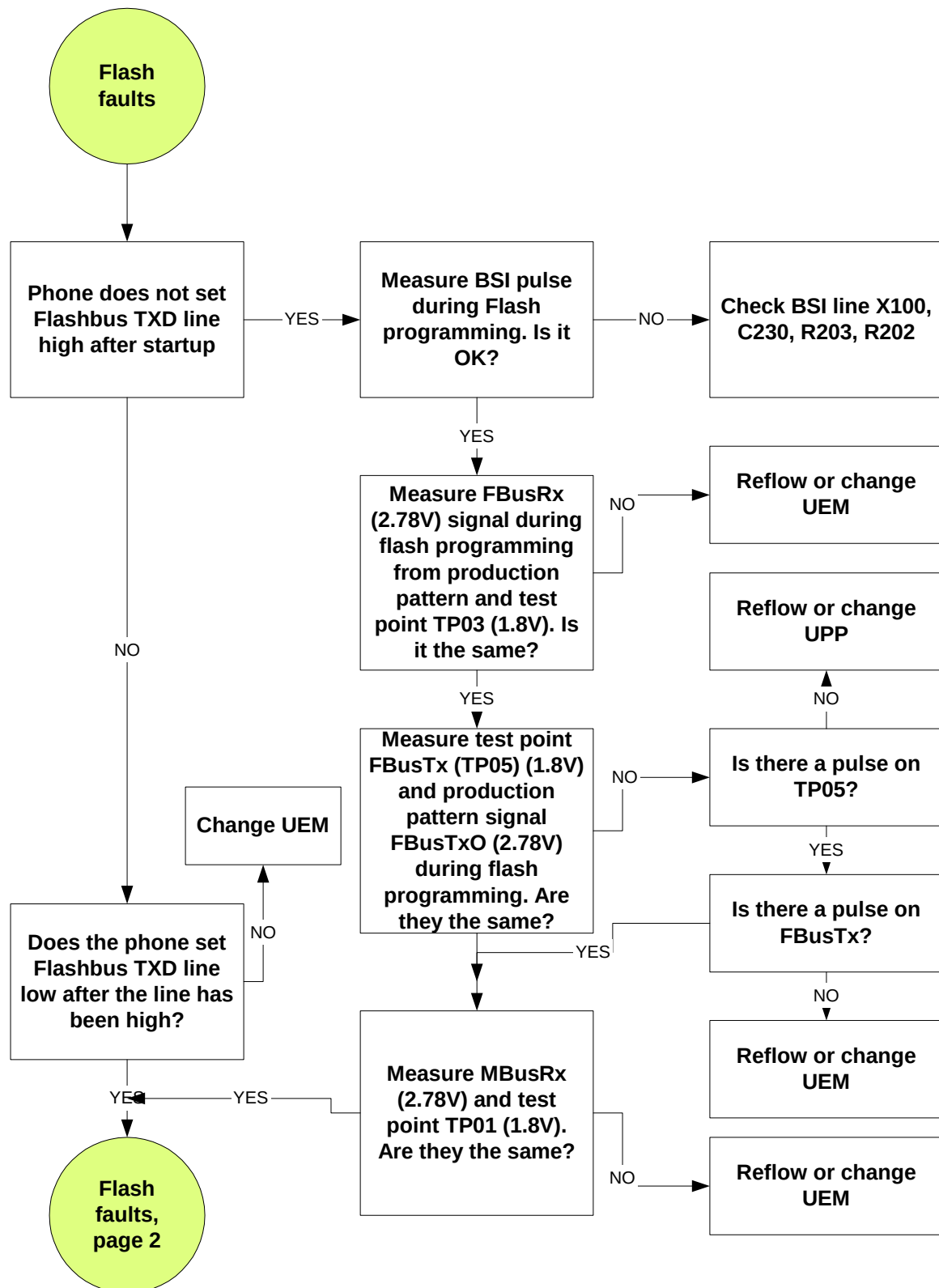


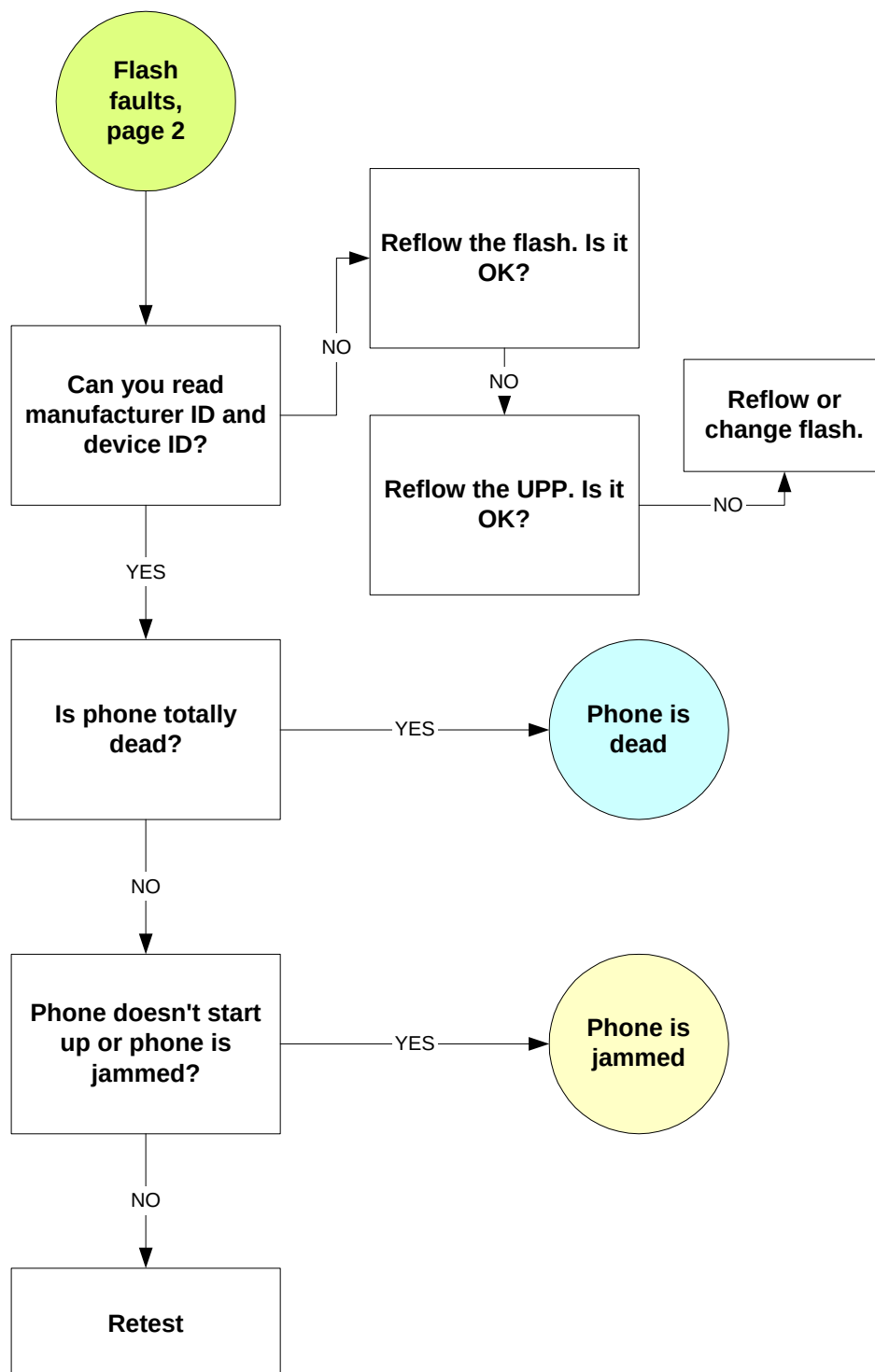


## Phone is Totally Dead

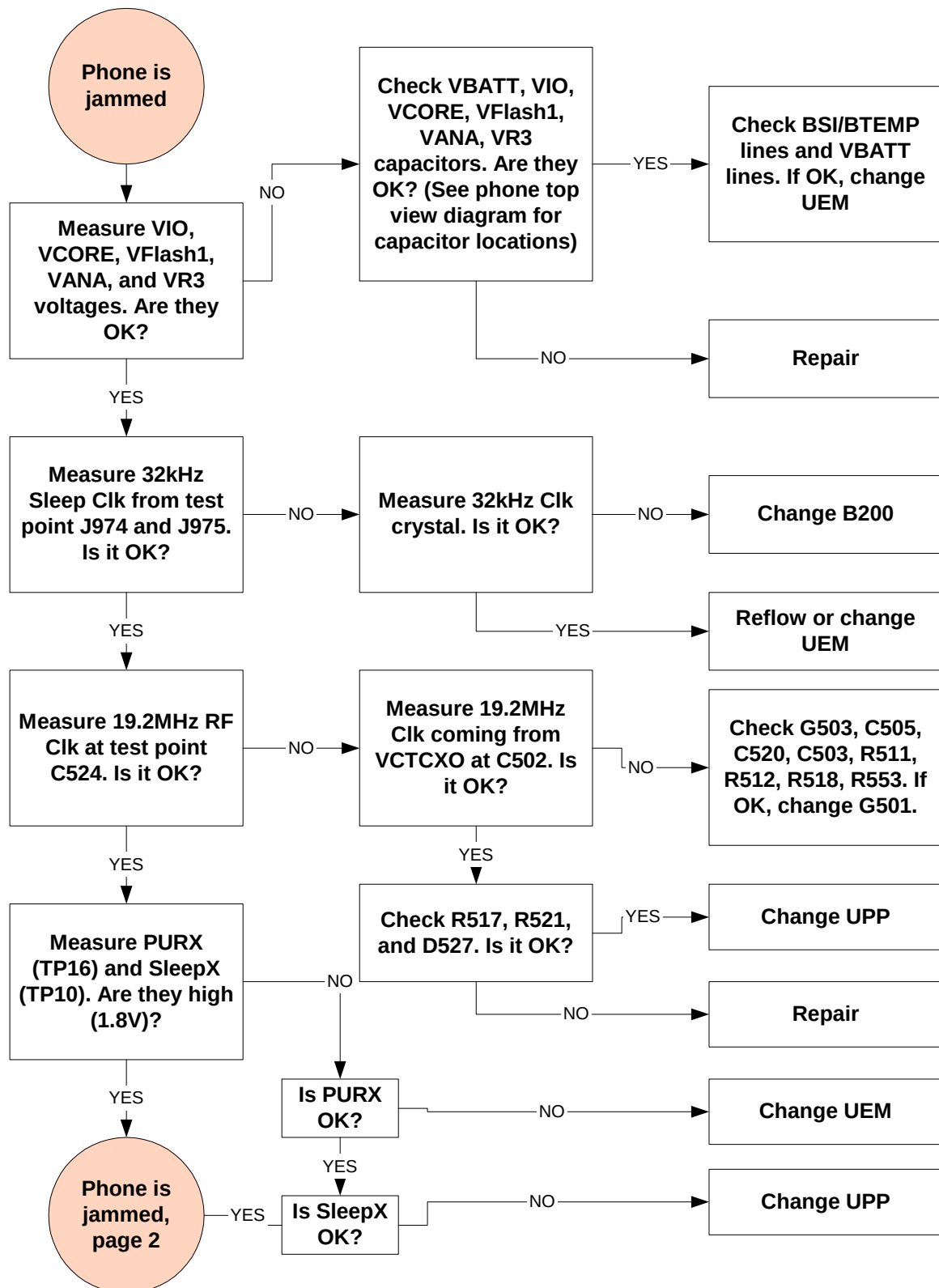


## Flash Programming Does Not Work

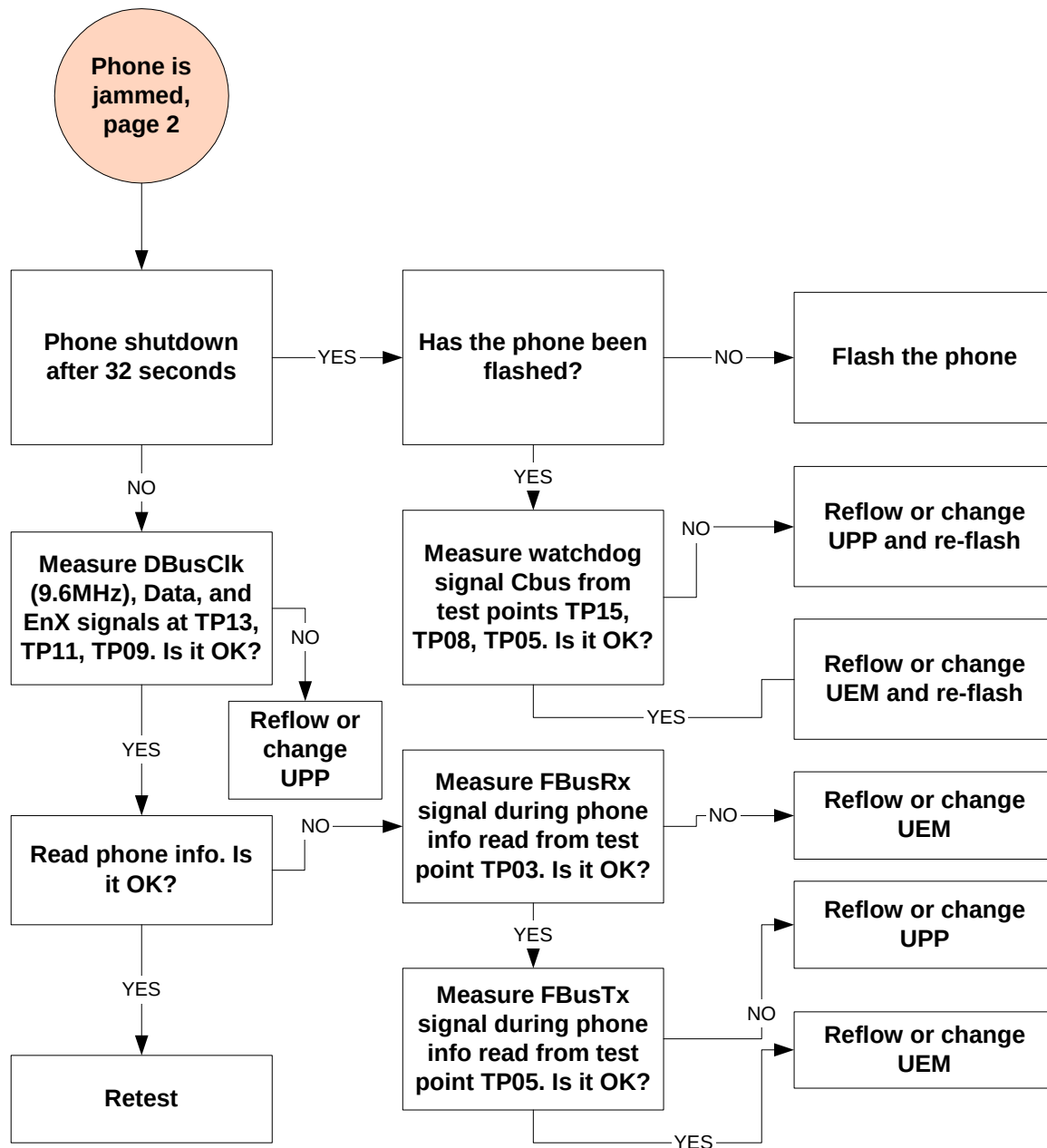




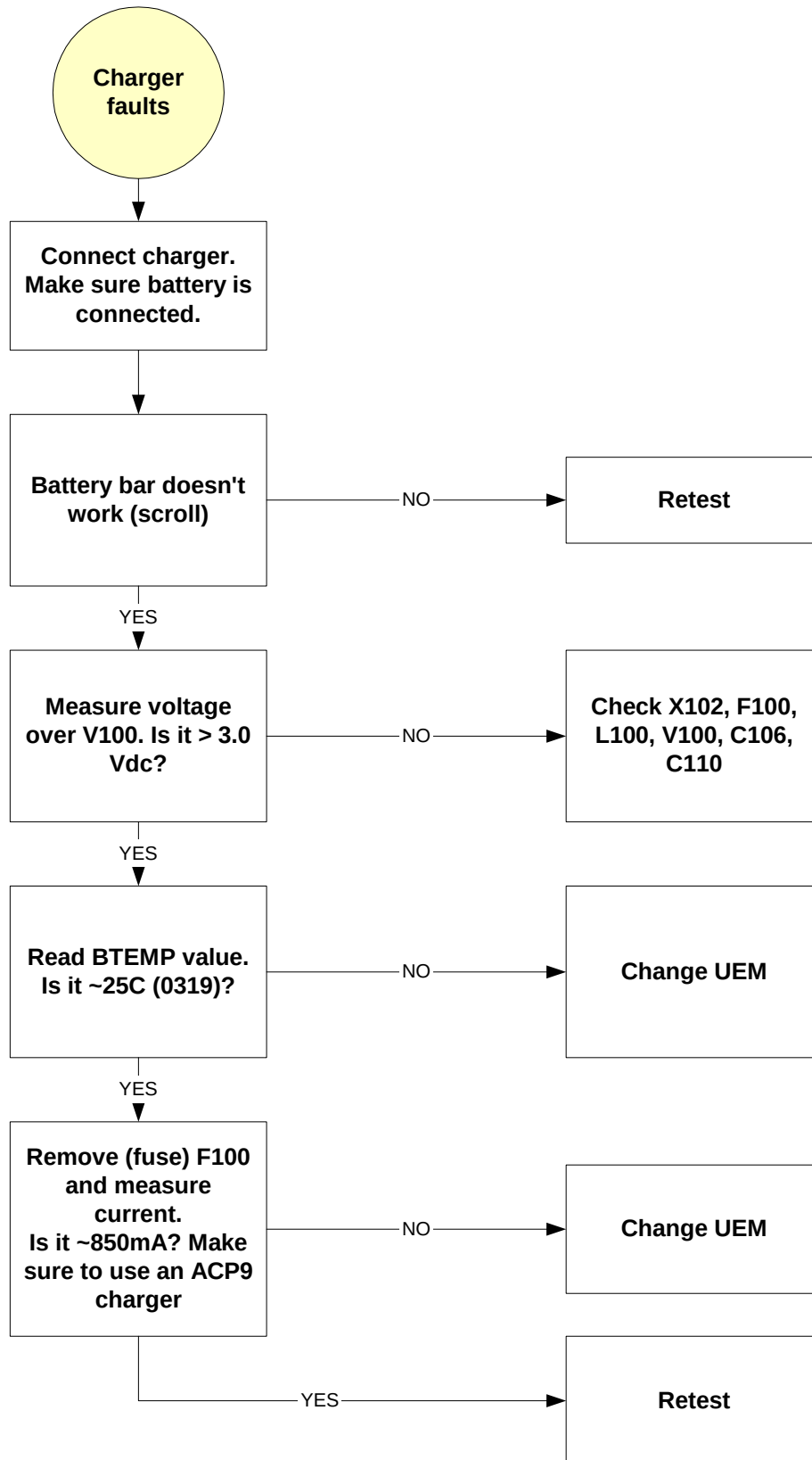
## Phone is Jammed



## Power Does Not Stay on or the Phone is Jammed

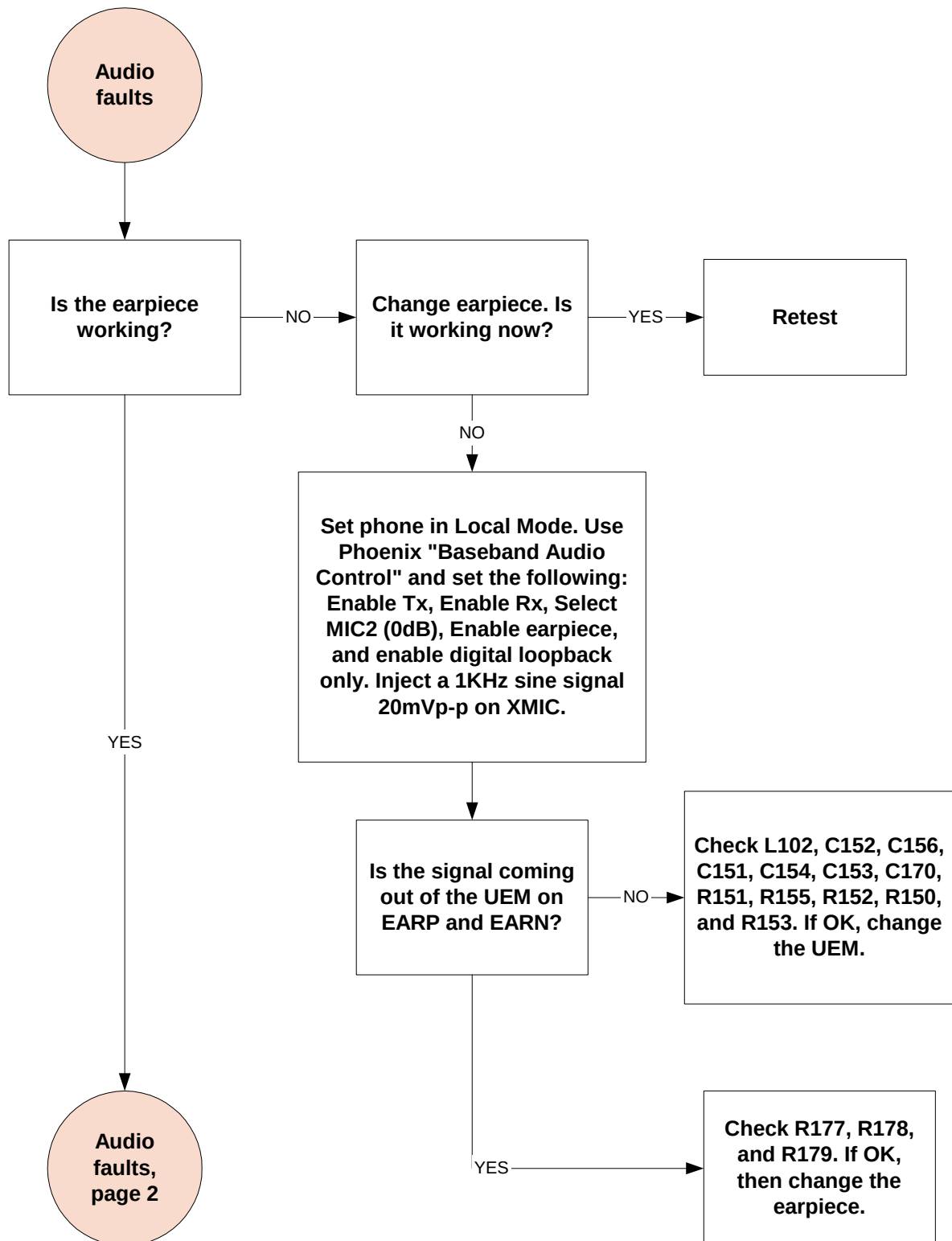


## Charger Faults

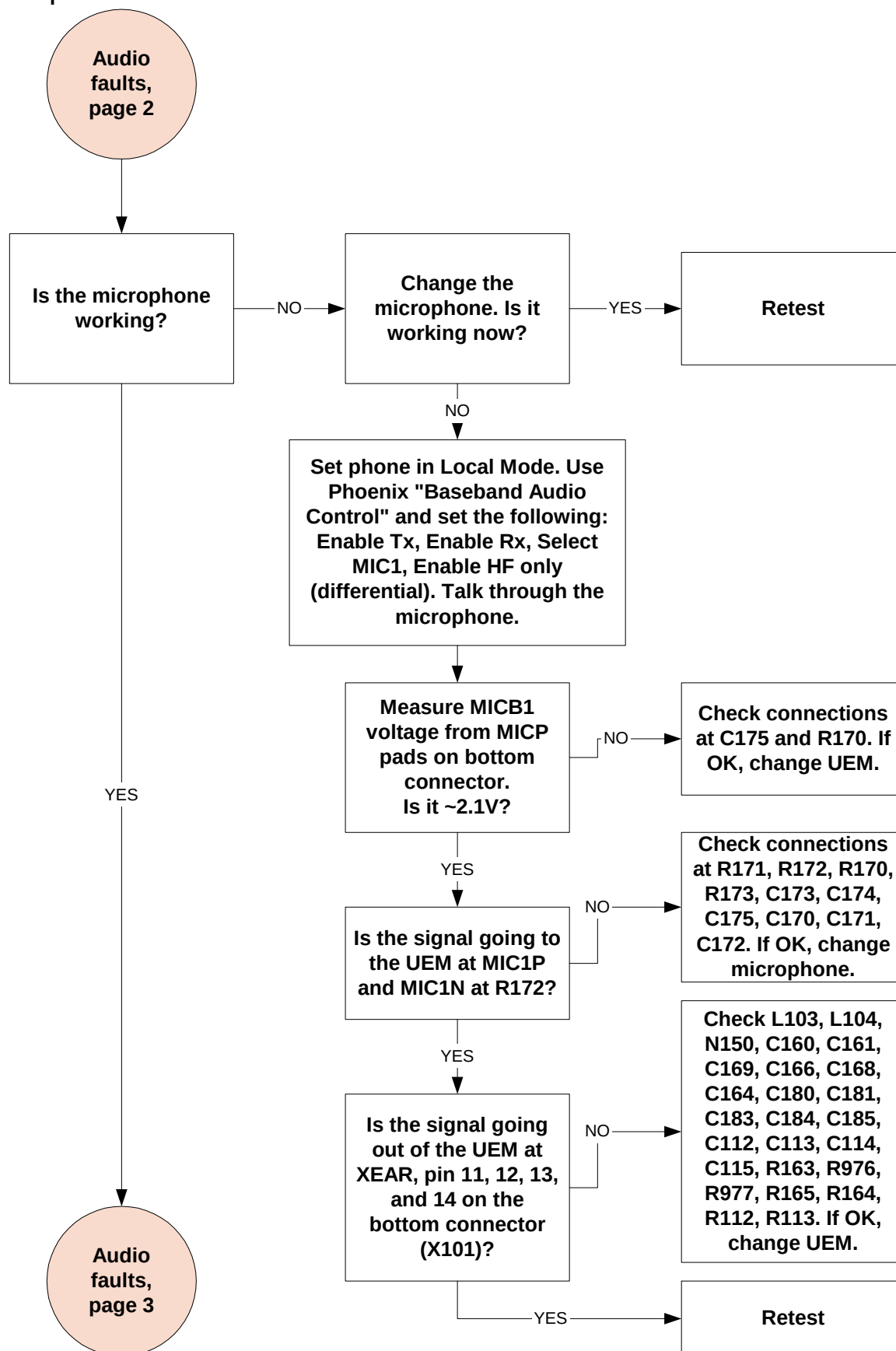


## Audio Faults

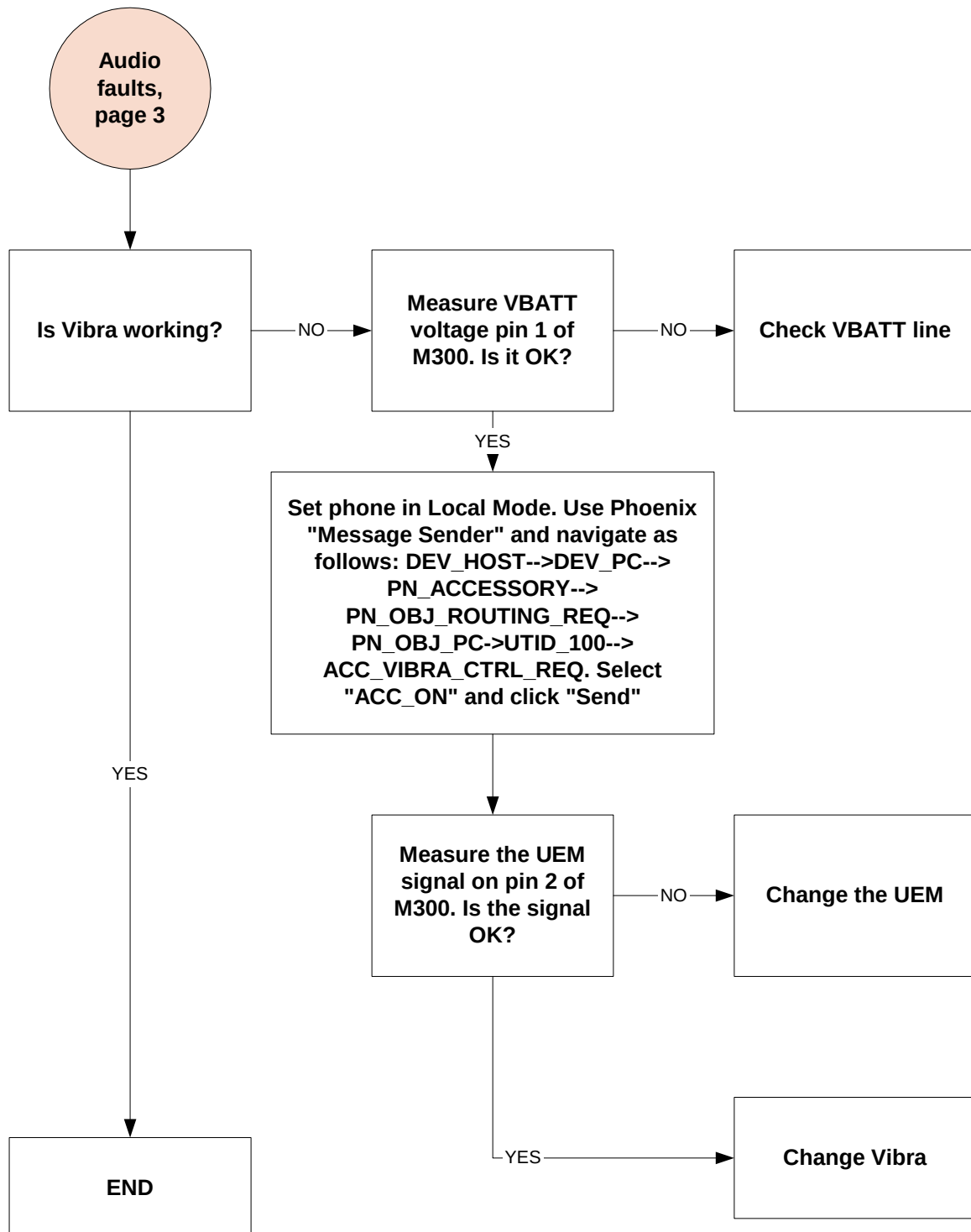
### Earpiece



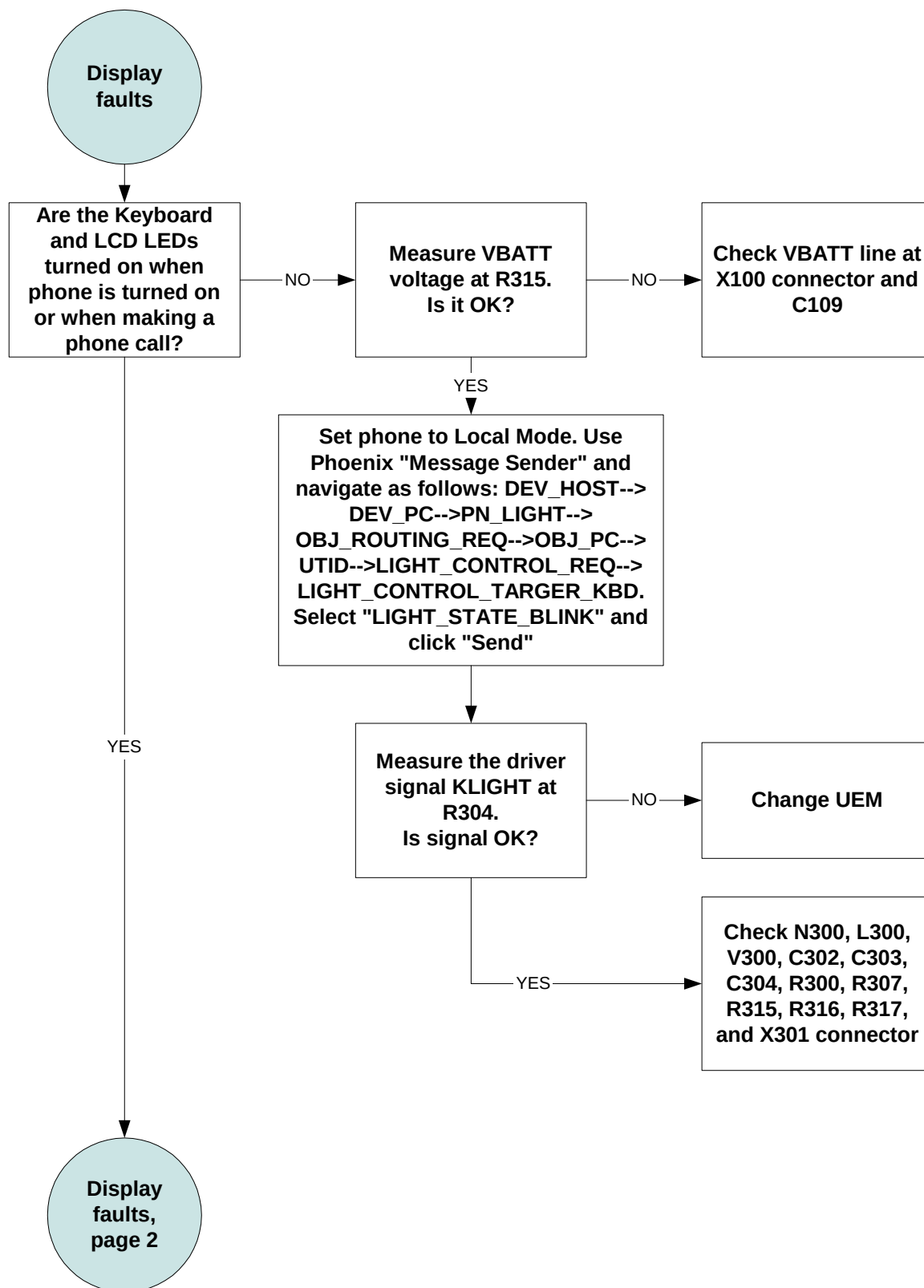
## Microphone

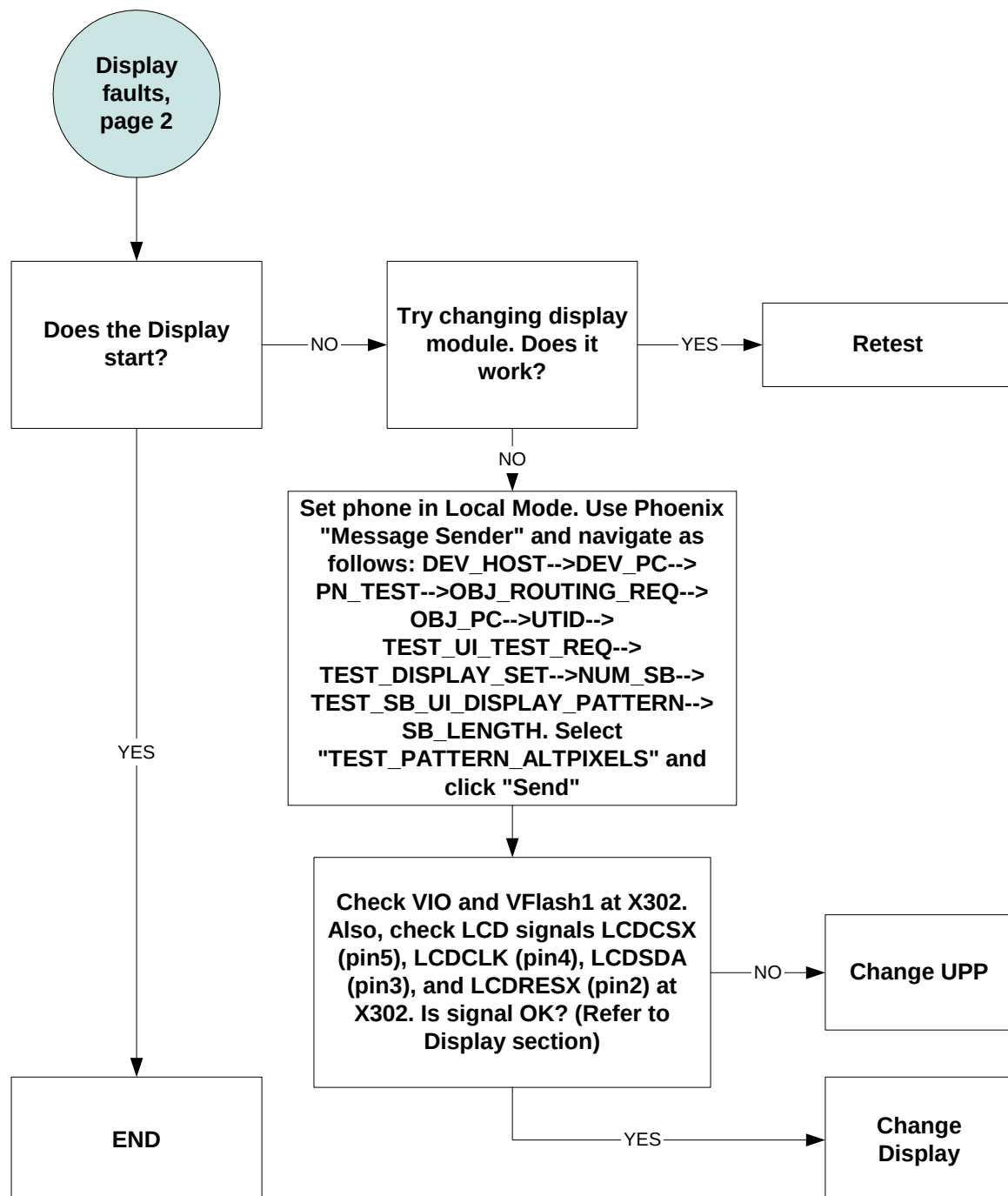


## Vibra



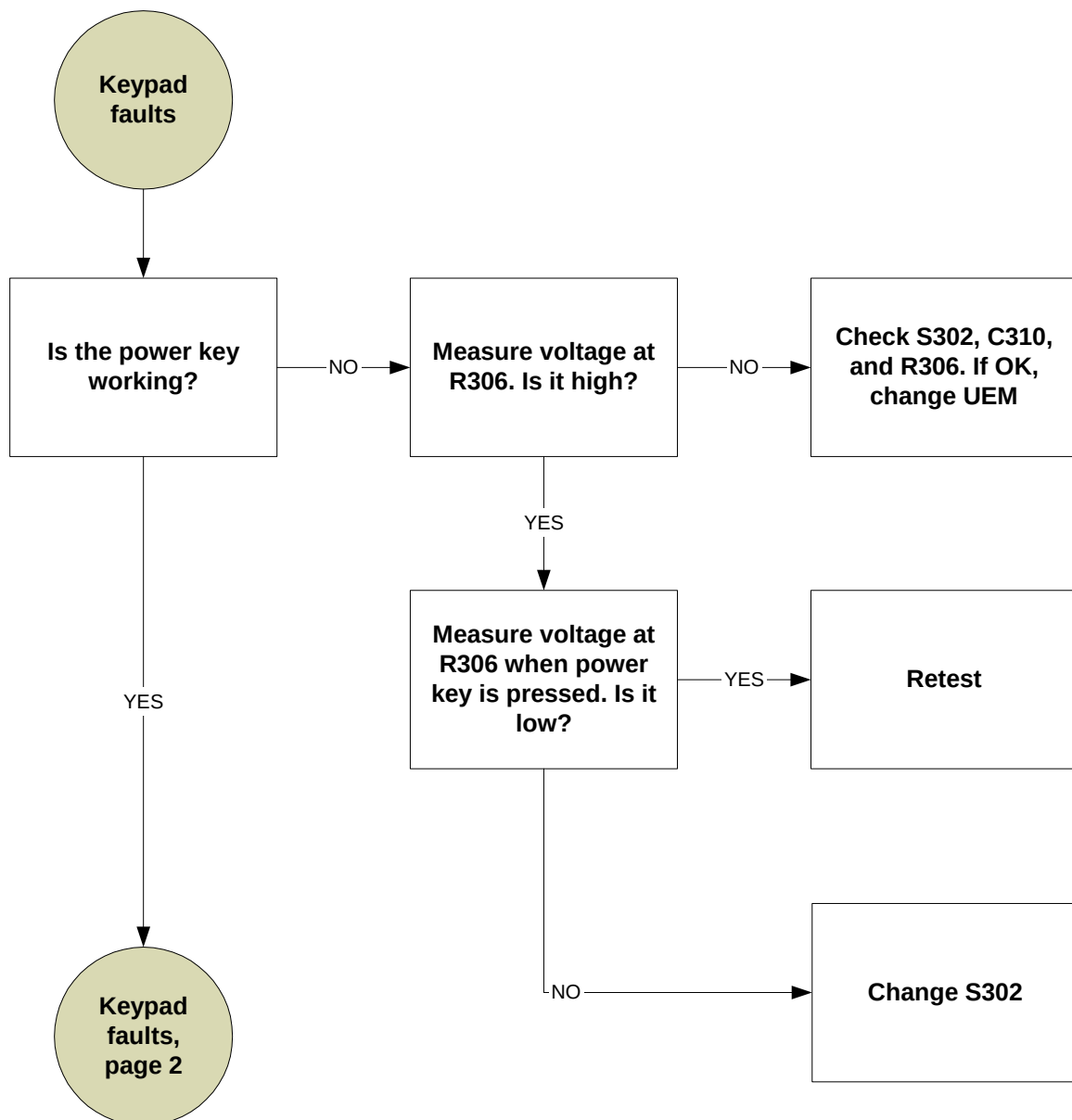
## Display Faults



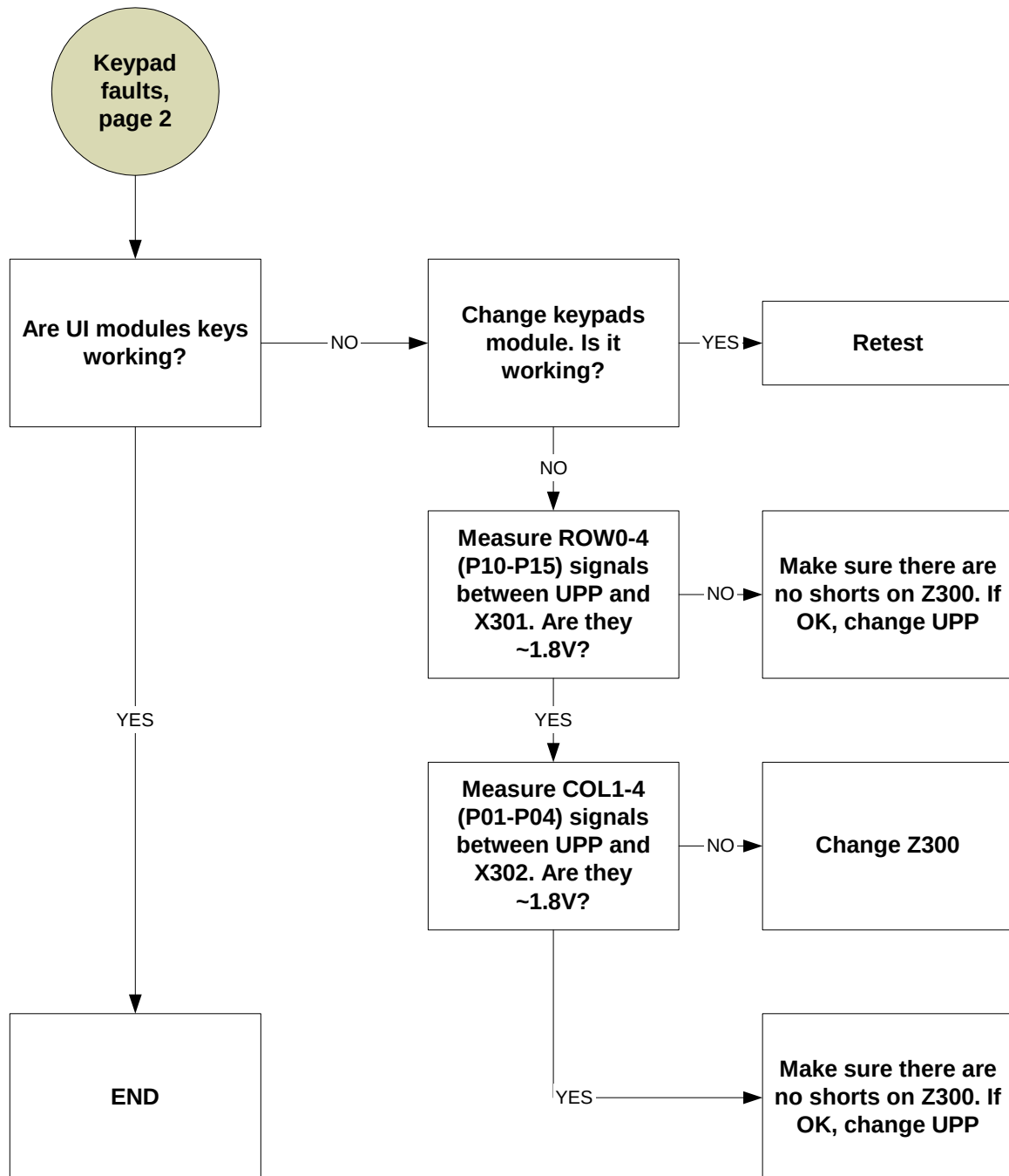


## Keypad Faults

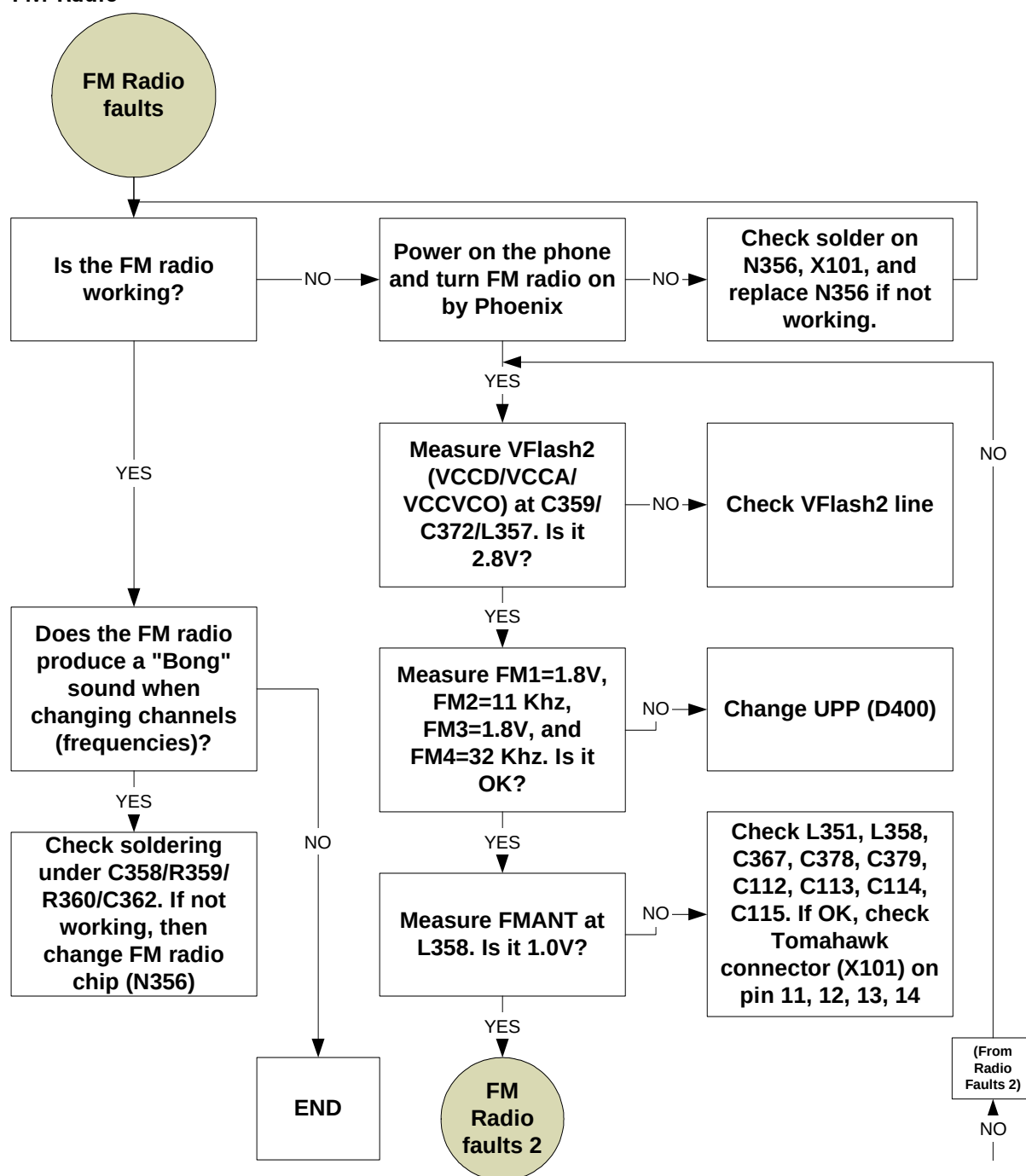
### Power Key

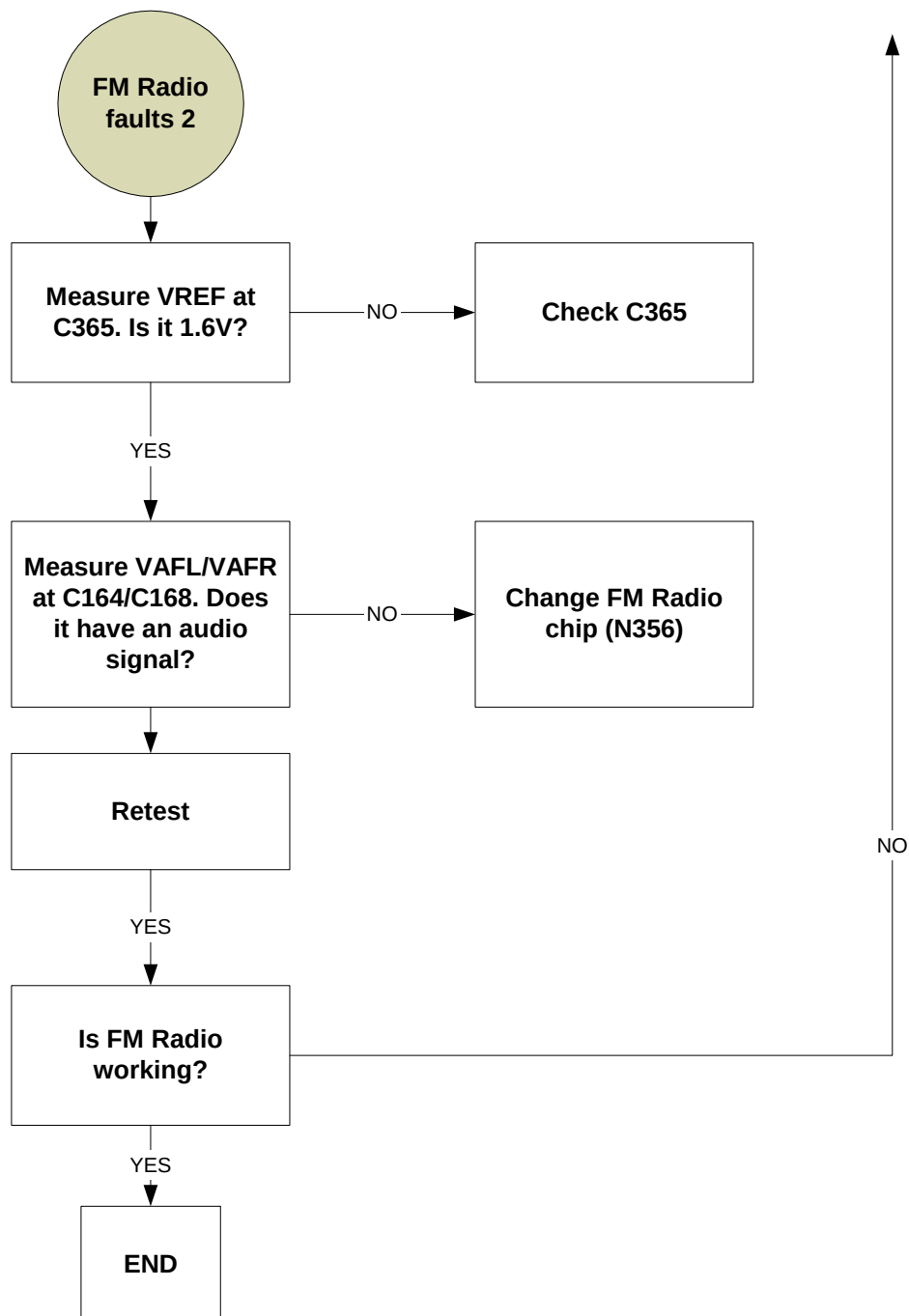


UI Modules

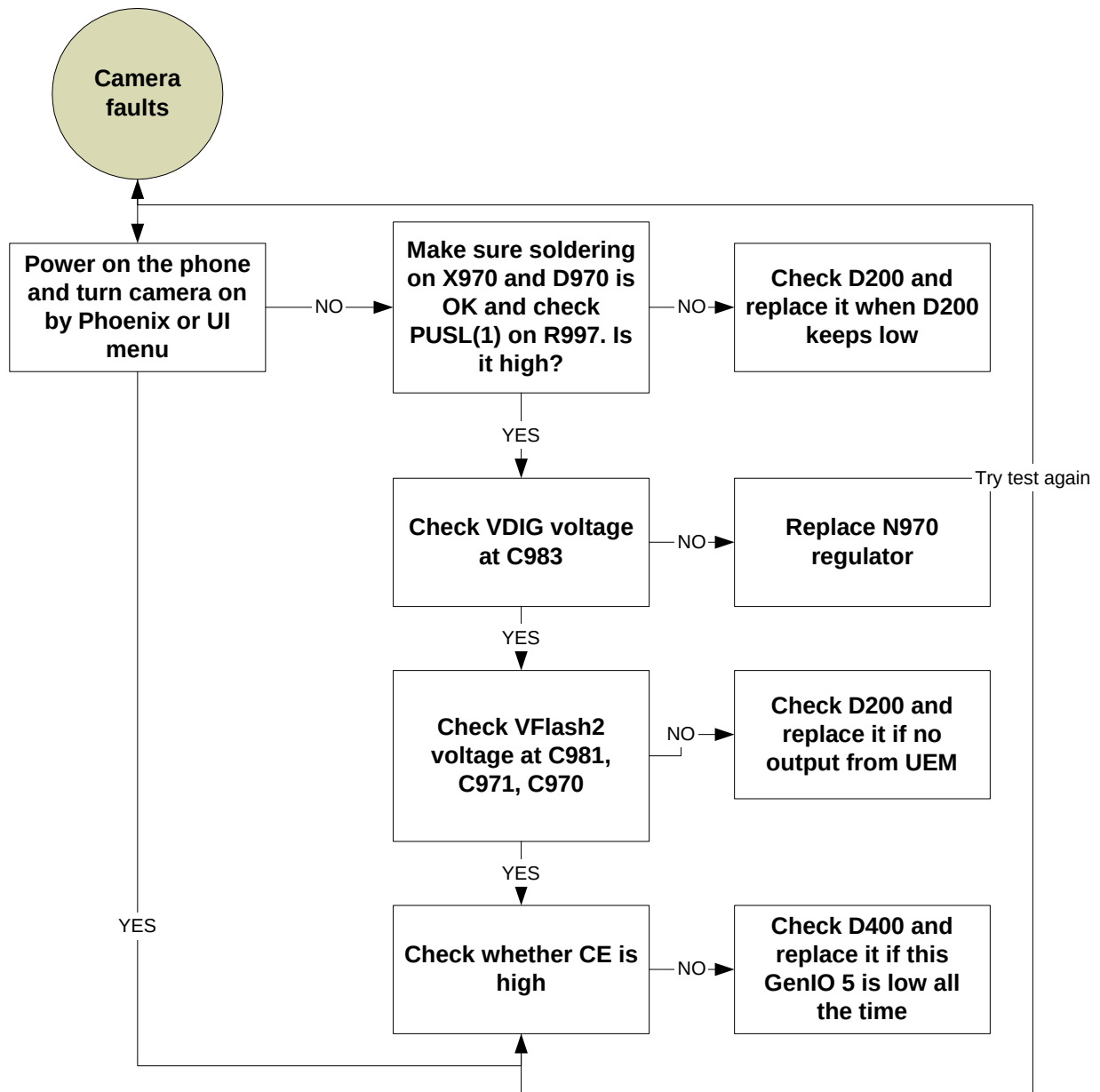


## FM Radio

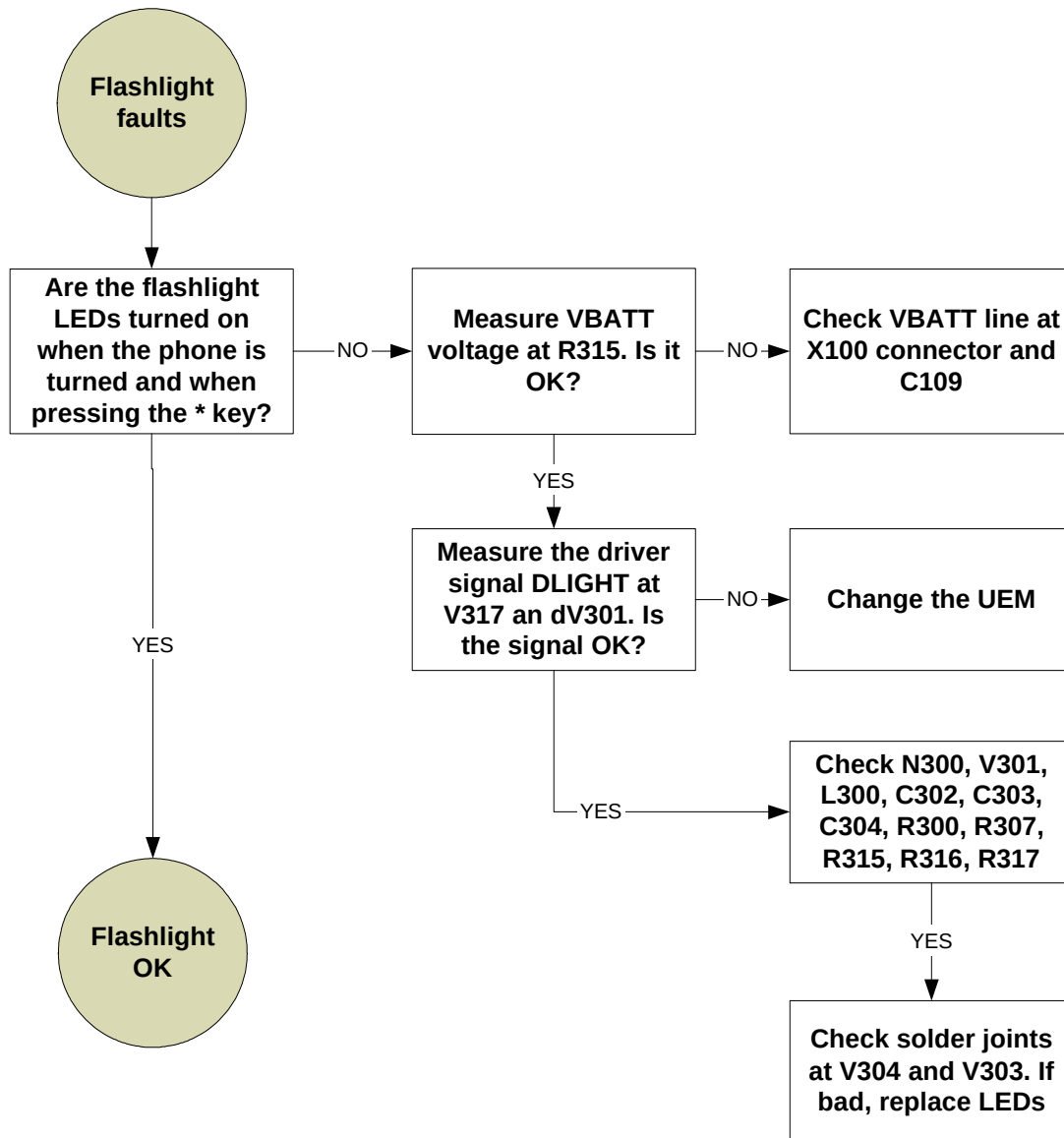




## Camera



## Flashlight



## GPS Module

### Overview

The GPS circuitry utilizes RF signals from satellites stationed in geosynchronous orbit to determine longitude and latitude of the handset. The GPS circuitry is completely separate from the CE circuitry and is located almost exclusively on the secondary side of the PWB underneath the display module (see Figure 38).

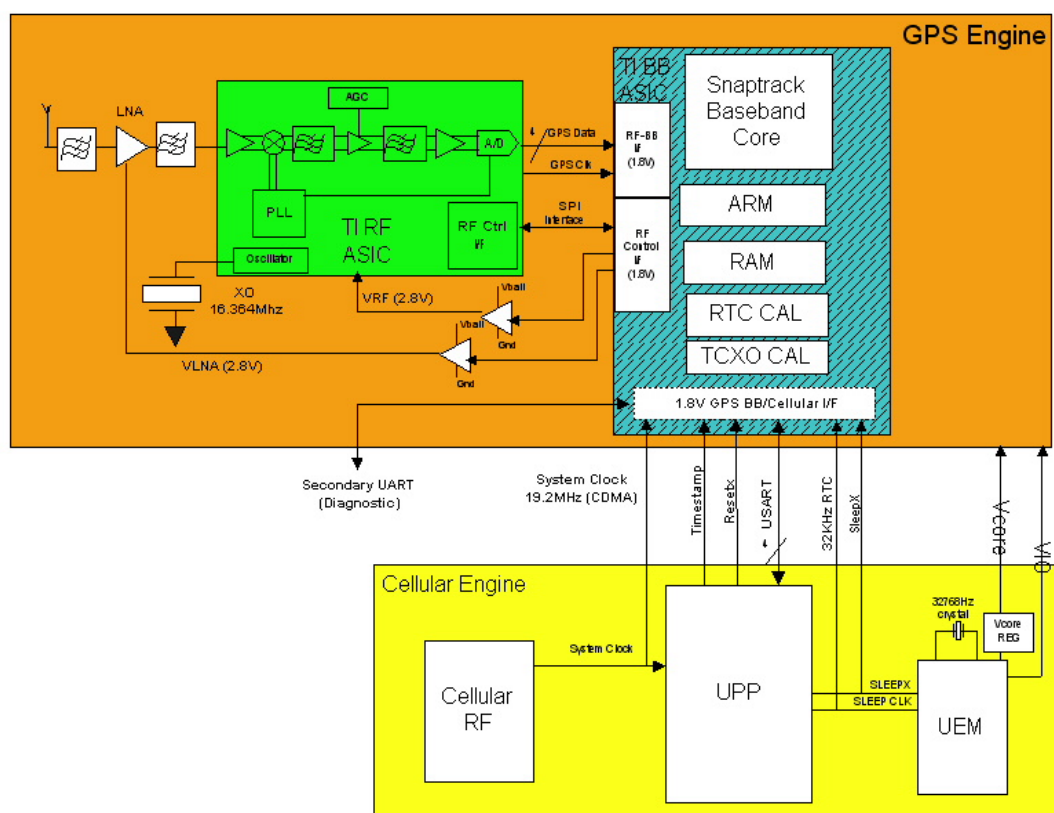


Figure 38: GPS block diagram

The basic GPS BB troubleshooting method is to put the GE and CE in the proper mode and check to make sure that necessary inputs from the CE are good (power, clock, etc.). Then, ensure that these inputs produce the proper outputs. Because of the large level of integration (most functionality is contained in the two ASIC chips), the amount of diagnostics one is able to do is limited.

Prior to performing diagnostics, perform a visual inspection on the GPS circuitry to see if the problem is physical (dislodged parts, corrosion, poor solder joints, etc.)

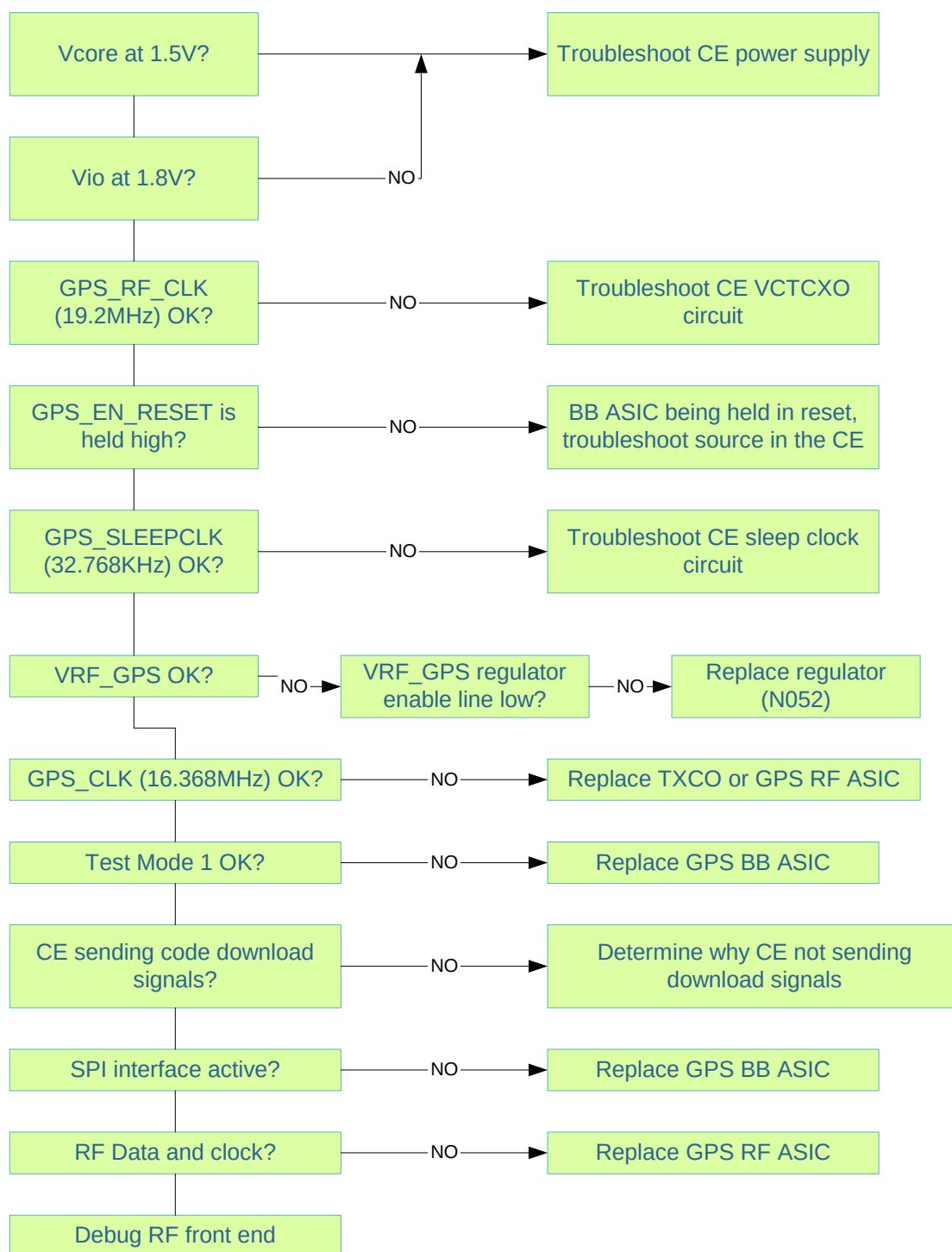


Figure 39: GPS troubleshooting flowchart